

Lenovo C340/C440 M0B(SDV) Schematic

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PCB Version : XXXXXXXXXXXXXXX

XTAL LIST

	PARTS	DIP/SMT	Frequency	PPM	CL
1	X1	SMT	25MHz	±20	10pF/10pF
2	X2	SMT	32.768KHz	±20	7pF/7pF
3	X3	SMT	25MHz	±20	10pF/10pF

SATA LIST

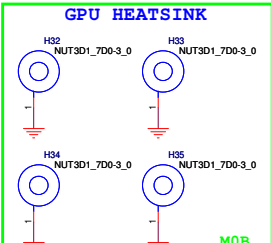
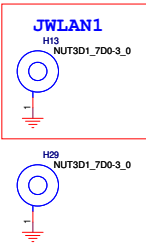
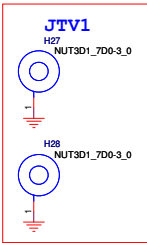
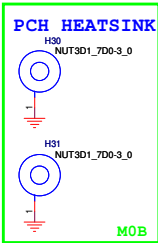
PORT	NET NAME	FUNCTION
SATA_TX0P/N	SATA_TX0P/N	SATA HDD
SATA_RX0P/N	SATA_RX0P/N	
SATA_TX1P/N	SATA_TX1P/N	SATA ODD
SATA_RX1P/N	SATA_RX1P/N	

USB LIST

PORT	NET NAME	FUNCTION
USB PORT 0	USB0P/N	SIDE IO
USB PORT 1	USB1P/N	SIDE IO
USB PORT 2	USB2P/N	REAR IO
USB PORT 3	USB3P/N	REAR IO
USB PORT 4	USB4_WLAN_P/N	WLAN CARD
USB PORT 5	USB5_WEBCAM_P/N	WEBCAM
USB PORT 8	USB8_TV_P/N	TV CARD
USB PORT 11	USB11_TSCREEN_P/N	TOUCH SCREEN

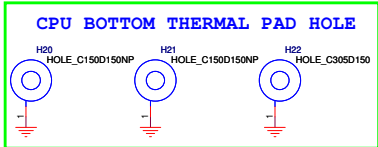
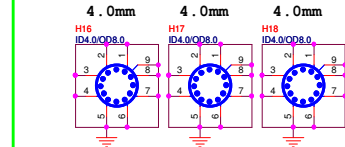
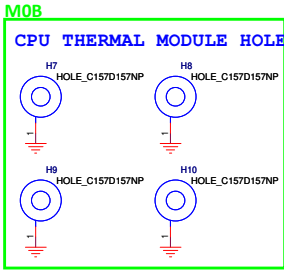
PCI-E LIST

PORT	NET NAME	FUNCTION
2	PCIE_USB3_TXP/N	USB3.0
2	PCIE_USB3_RXP/N	
3	PCIE_LAN_TXP/N	GIGA LAN
3	PCIE_LAN_RXP/N	
4	PCIE_CR_TXP/N	CARD READER
4	PCIE_CR_RXP/N	
5	PCIE_TV_TXP/N	TV CARD
5	PCIE_TV_RXP/N	
6	PCIE_WLAN_TXP/N	WLAN CARD
6	PCIE_WLAN_RXP/N	



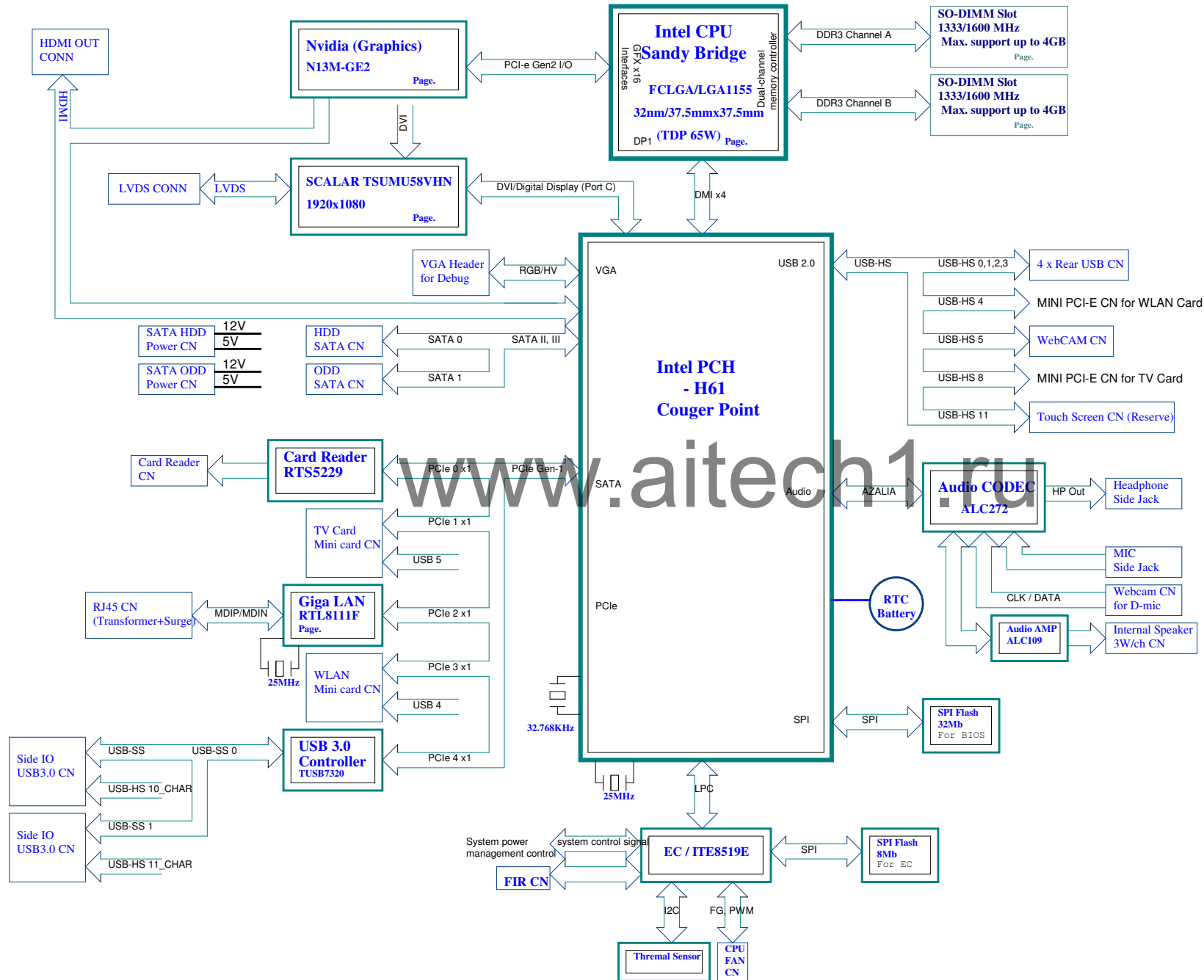
POWER STATES

STATE	VOTAGE	S0	S3	S5	G3
PCH_SLP_S3#	-	HIGH	LOW	LOW	LOW
PCH_SLP_S5#	-	HIGH	HIGH	LOW	LOW
S5_PWR_ON	-	HIGH	HIGH	HIGH	LOW
+VBAT_IN	+3.3V	O	O	O	O
+VIN	+19V	O	O	O	X
+3V_LDO/+5V_LDO	+3.3V/+5V	O	O	O	X
+3V_S5	+3.3V	O	O	O	X
+5V_S5	+5V	O	O	O	X
+5V_S3	+5V	O	O	X	X
+3V_S3	+3.3V	O	O	X	X
+1.1V_S3	+1.1V	O	O	X	X
+1.5V_S3	+1.5V	O	O	X	X
+MEM_VTT	+0.75V	O	X	X	X
+3V_S0/+5V_S0	+3.3V/+5V	O	X	X	X
+12V_S0	+12V	O	X	X	X
+1.8V_S0	+1.8V	O	X	X	X
+1.5V_S0	+1.5V	O	X	X	X
+1.05V_S0	+1.05V	O	X	X	X
+CPU_VCCIO	+1.0V	O	X	X	X
+0.85V_S0	+0.85V	O	X	X	X
+CPU_AXG	SVC/SVD	O	X	X	X
+CPU_VCC	SVC/SVD	O	X	X	X



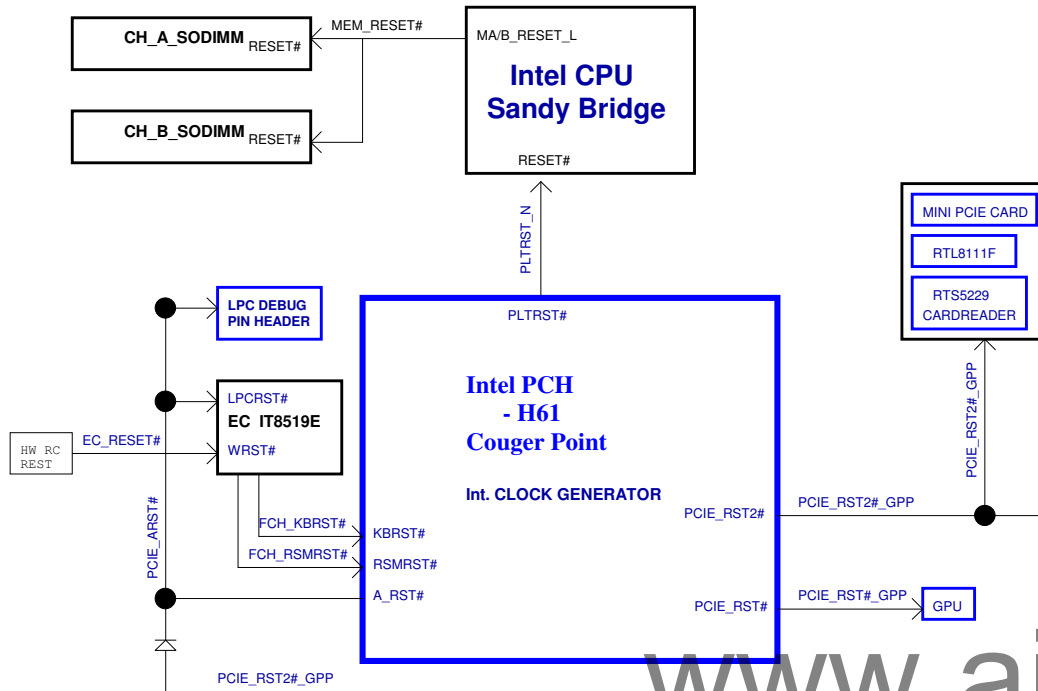
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Circuit diagram NO.	T&I MODEL	C340	Rev	X02
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Thursday, February 23, 2012	Sheet	1 of 45	<remark>

C340/C440

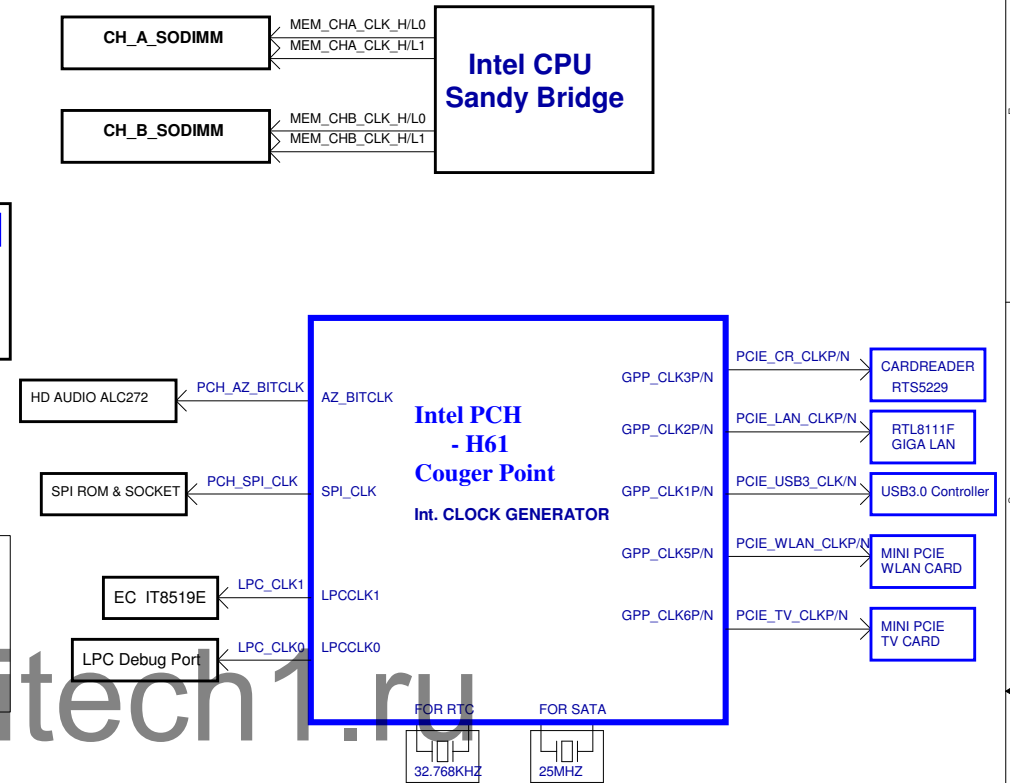


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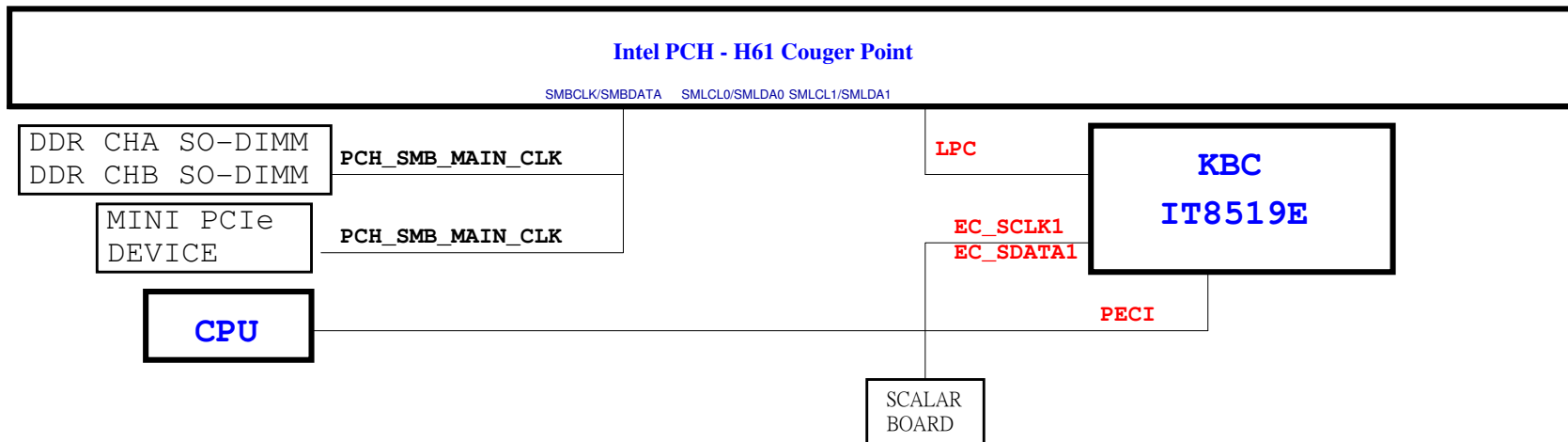
RESET Block Diagram



INTERNAL CLOCK MODE

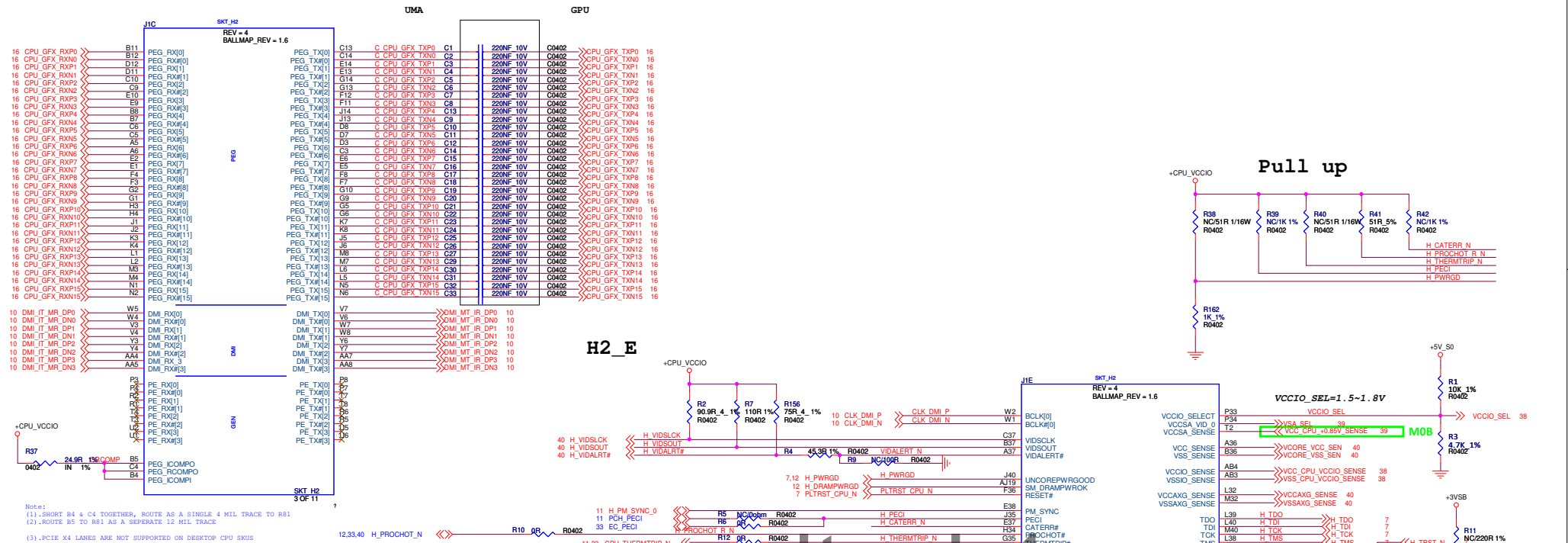


SM Bus MAP

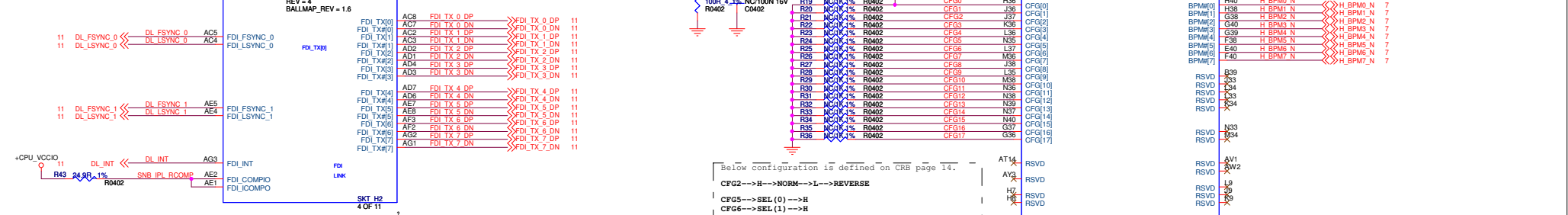


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Date	Thursday, February 23, 2012	Sheet	3 of 45		

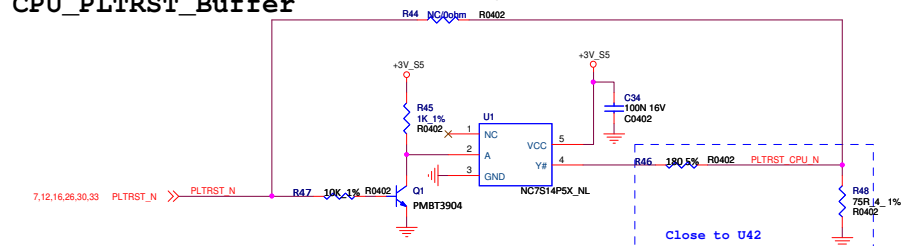
PCIEX16 & DMI



FDI

CPU PLTRST Buffer^I

If PLT_RST driver current enough. need to use buffer



Below configuration is defined on CRB page 14

CFG2-->H-->NORM-->L-->REVERSE

CFG5-->SEL(0)-->H

```
CFG6-->SEL(1)-->H
```

1810

CFG5-->SEL(0)-->L

CFG6-->SEL(1)-->H
2Y8

TABLE 1

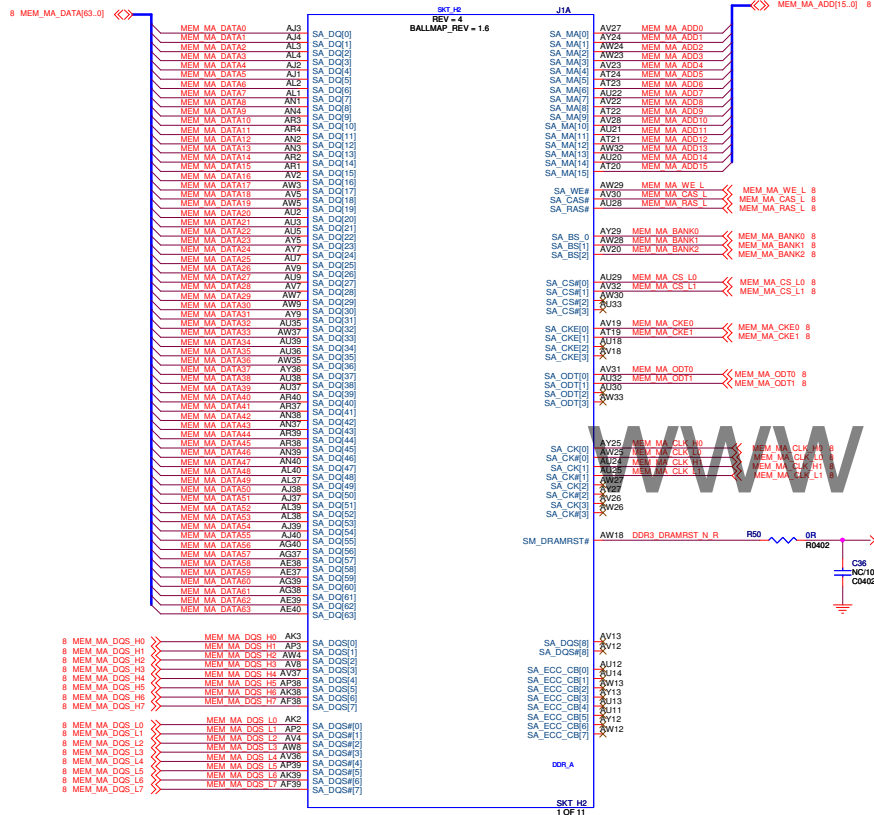
CFG5-->SEL(0)-->L

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| CFG6-->SEL(1)-->L
X8.X4.X2.X1
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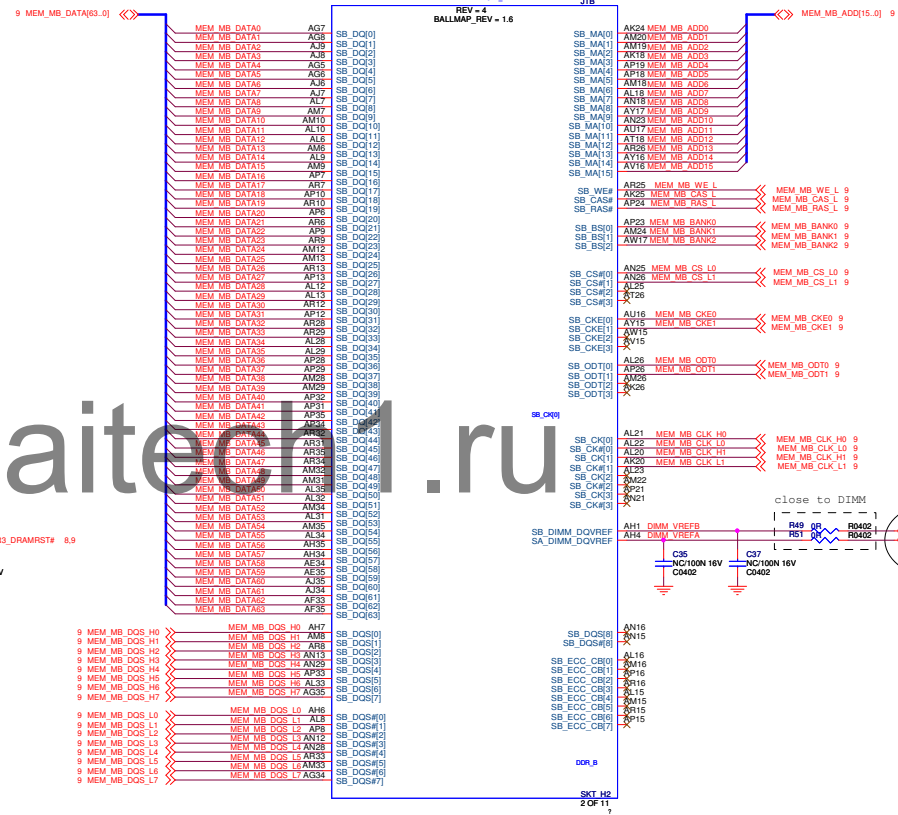
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Date	Thursday, February 23, 2012	Sheet	4 of 45		

Channel_A

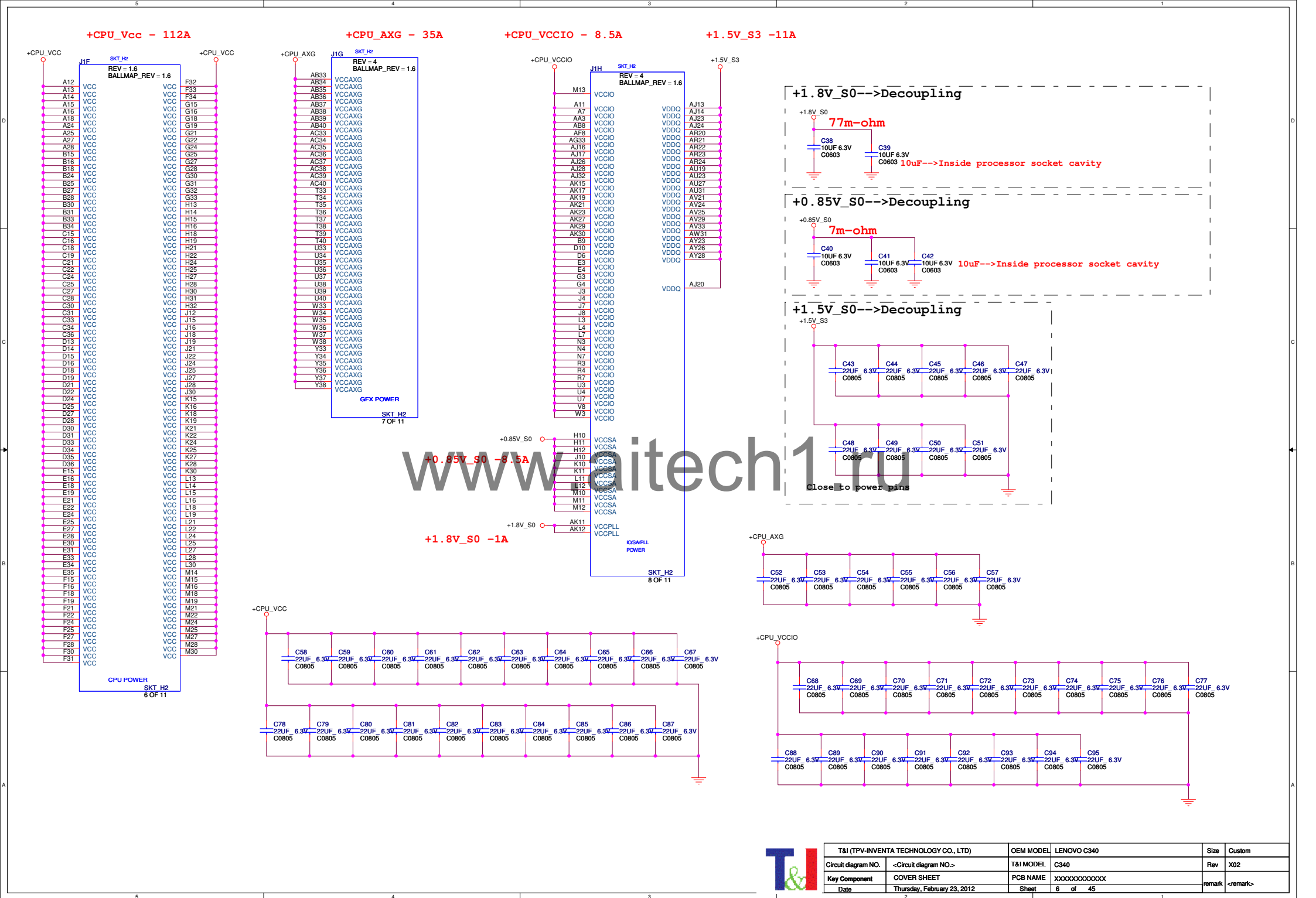


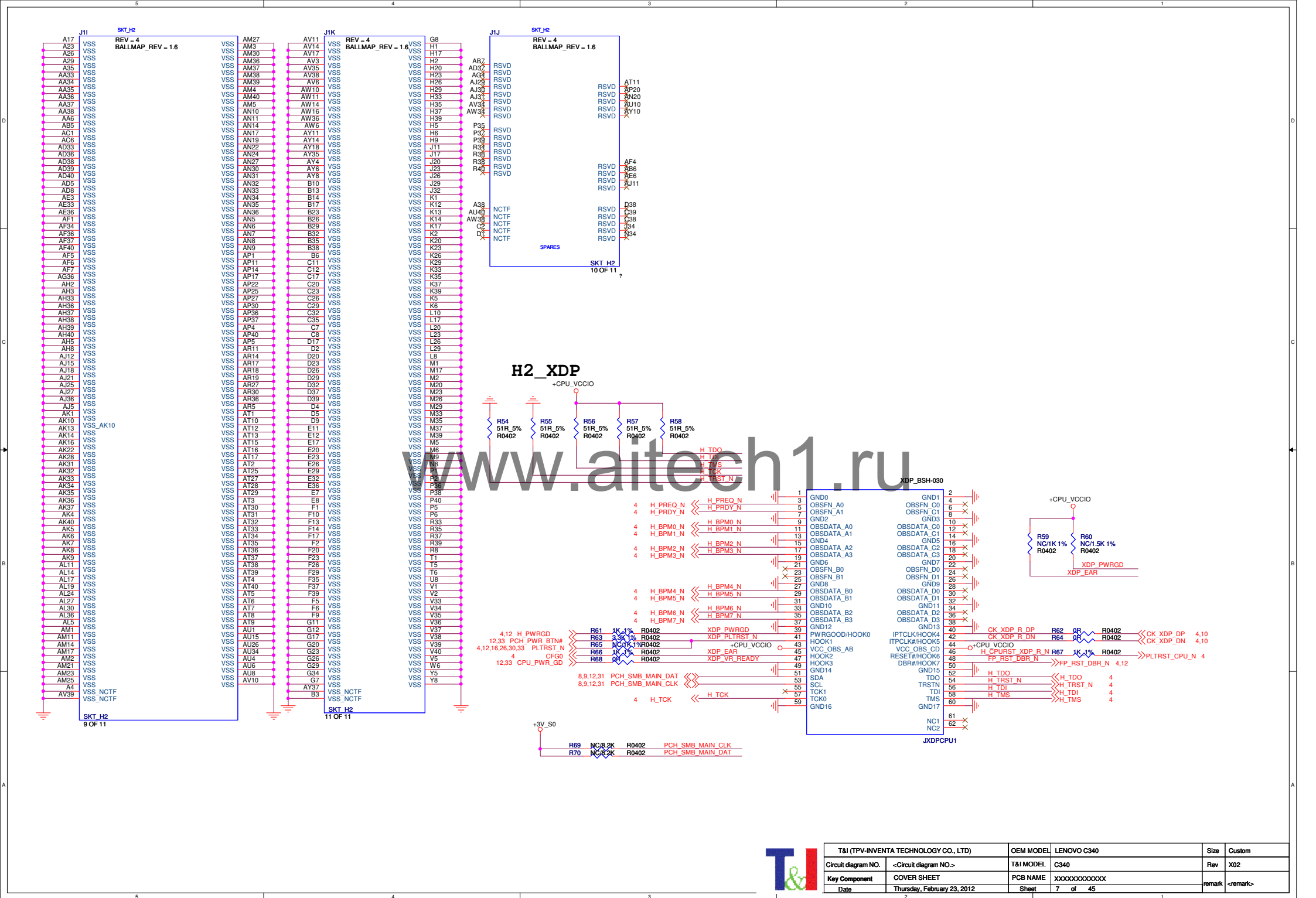
Channel_B



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T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL LENOVO C340		Size	Custom
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Date Thursday, February 23, 2012		Sheet 5 of 45			

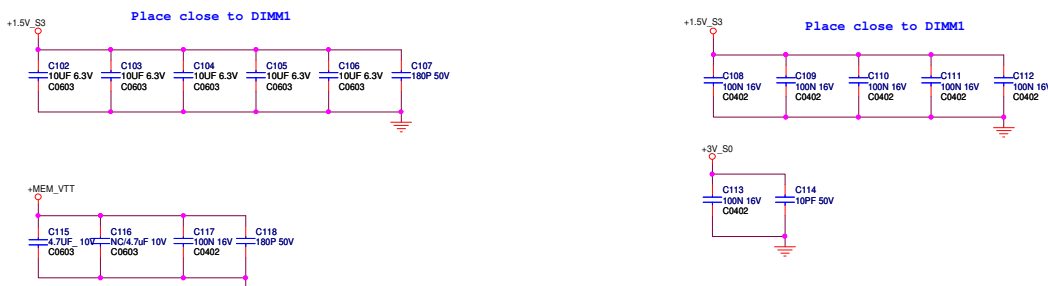
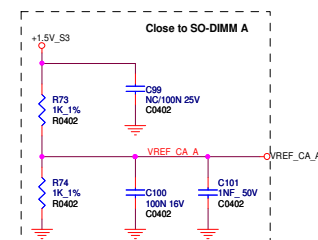
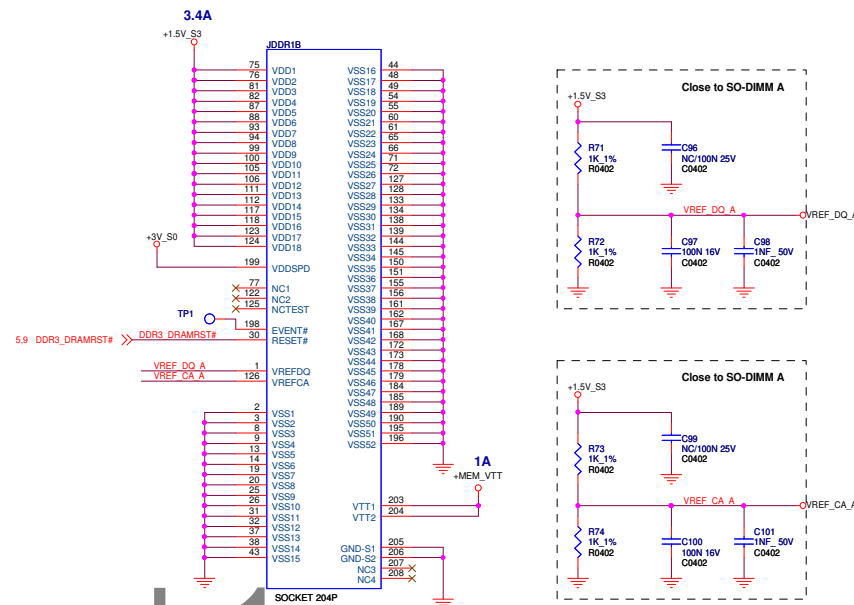





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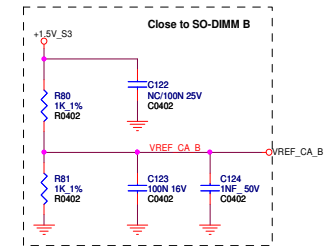
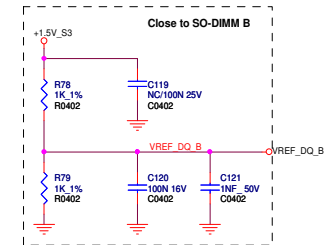
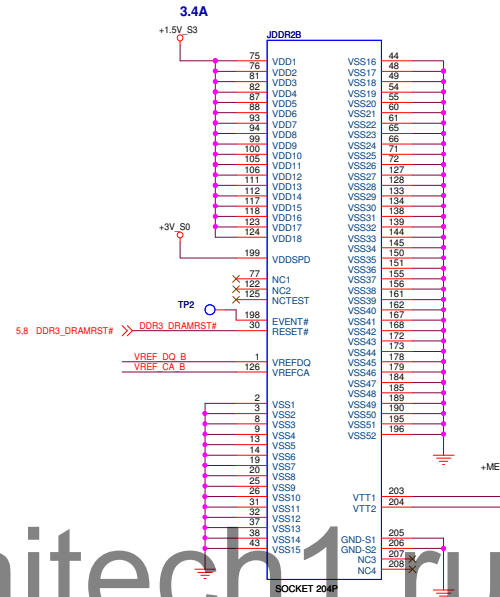
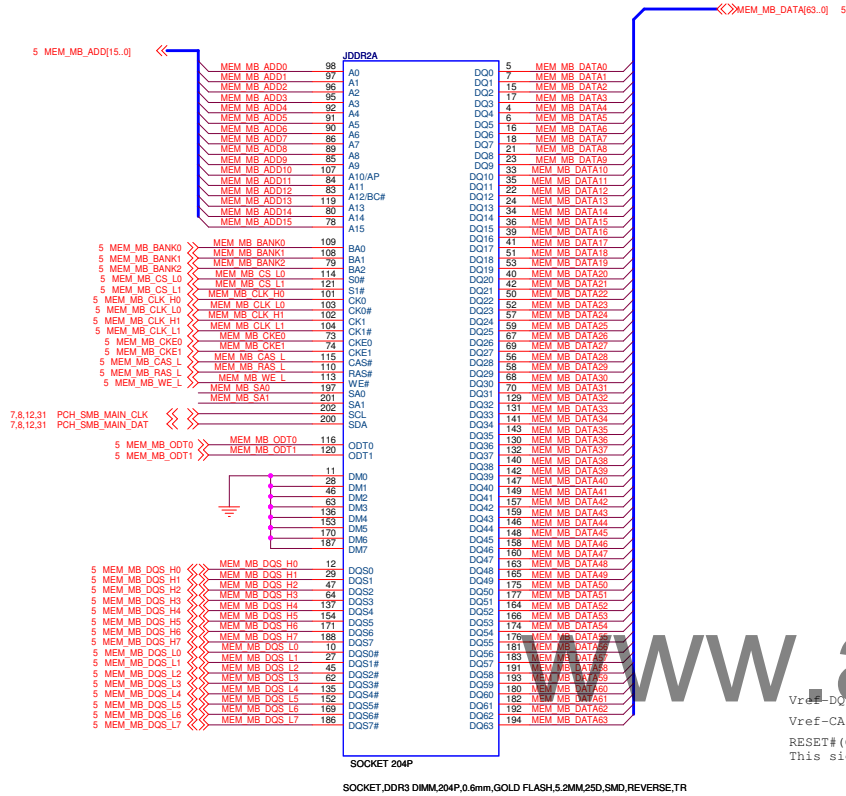
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Date	Thursday, February 23, 2012	Sheet	7 of 45		

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	T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
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	Key Component	COVER SHEET	PCB NAME	X000000000000X	remark	<remark>
	Date	Thursday, February 23, 2012	Sheet	8 of 45		

CHB DDR 5.2H(DIMM-2)

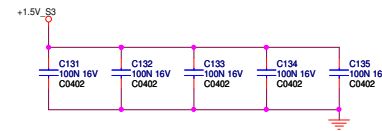
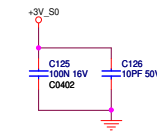
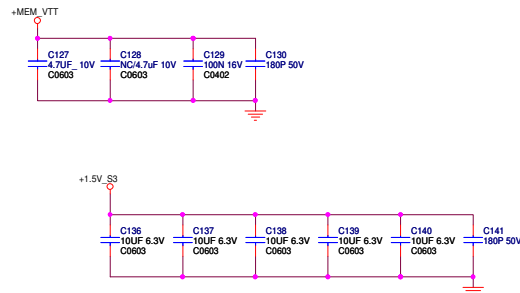
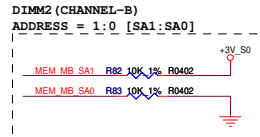


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Vref-DQ : Reference voltage for DQ0-DQ63, CB0-CB7 and PAR_IN. When in single ended mode used for DQS0-DQS7.

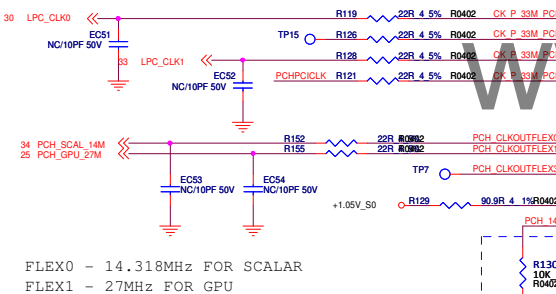
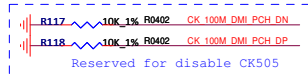
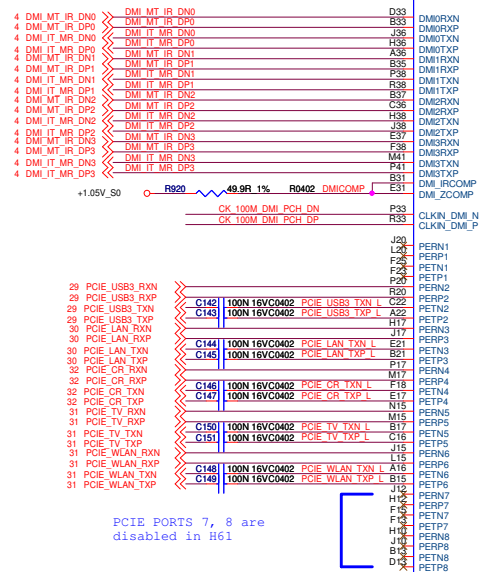
Vref-CA : Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW.
This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.



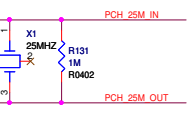
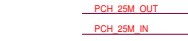
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Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Thursday, February 23, 2012	Sheet	9 of 45	<remark>

PCH DMI/PCIE/USB

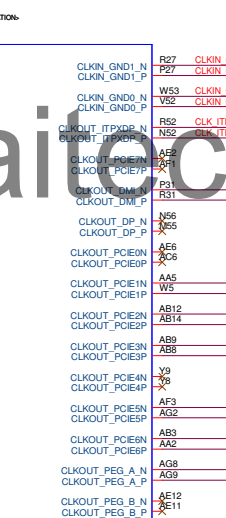
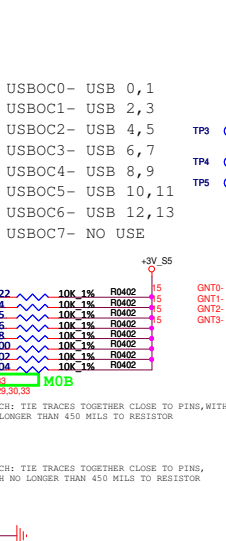
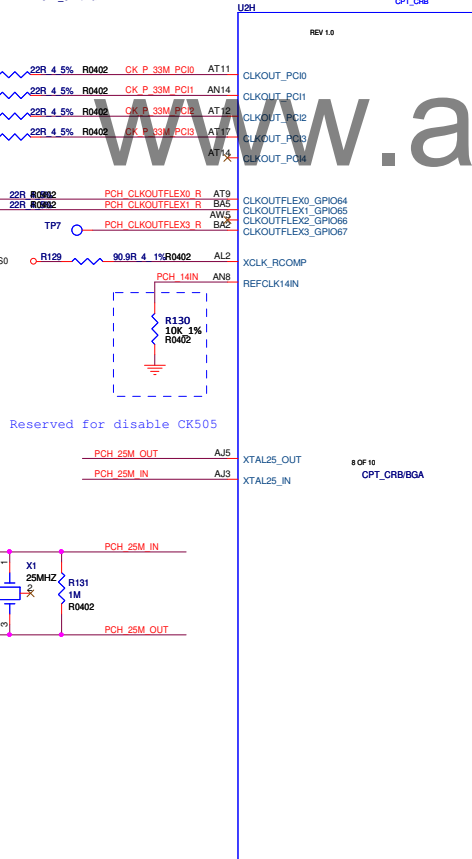


```
FLEX0 - 14.318MHz FOR SCALAR
FLEX1 - 27MHz FOR GPU
```

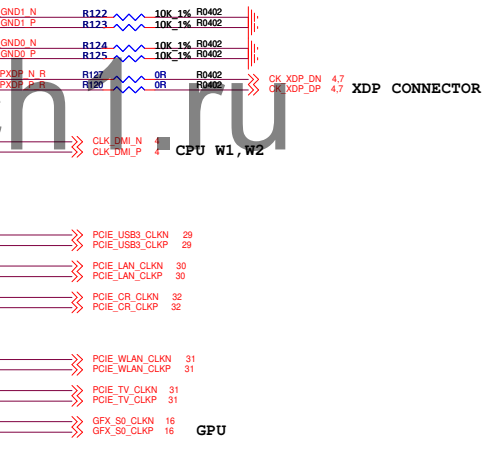
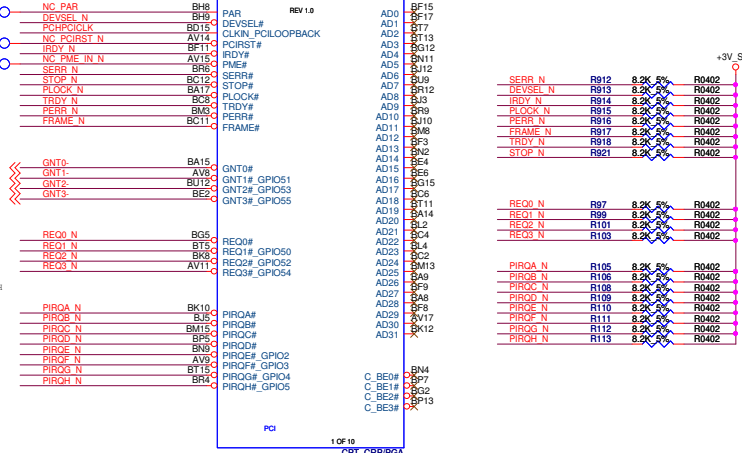
Reserved for disable CK505



PCH_Clock

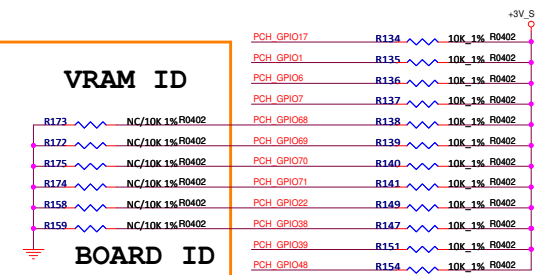


PCH_PCI



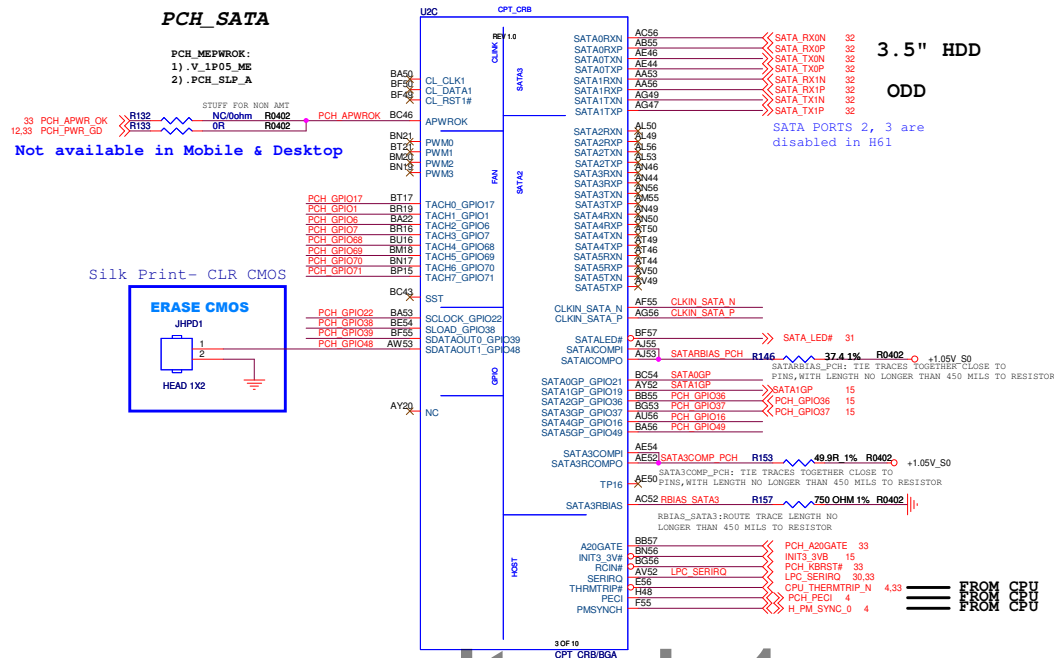
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Key Component		COVER SHEET		PCB NAME		XXXXXXXXXXXXXX		remark	
Date		Thursday, February 23, 2012		Sheet		10 of 45		<remark>	

CONFIG.	128M X 16		64M X 16	
VRAM TYPE	SS	HY	SS	HY
PCH_GPIO68	1	1	1	0
PCH_GPIO69	1	1	0	1
PCH_GPIO70	1	0	1	1
PCH_GPIO71	1	1	1	1

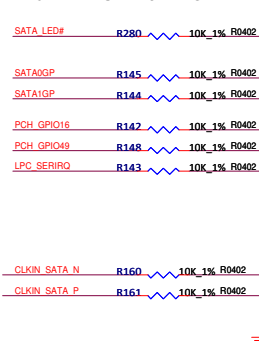


Pull HIGH for PCH

PCB_STAGE	ET	SDT	SIT
PCH_GPIO22	0	0	1
PCH_GPIO38	0	1	1

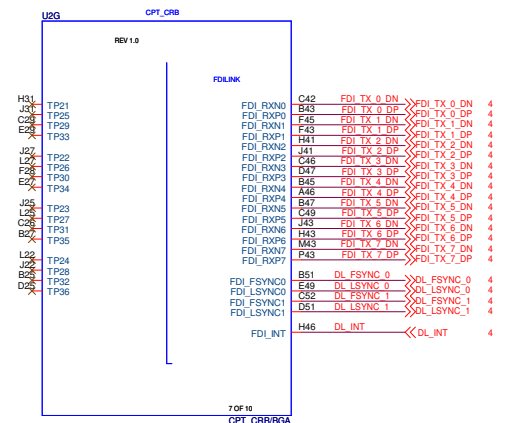
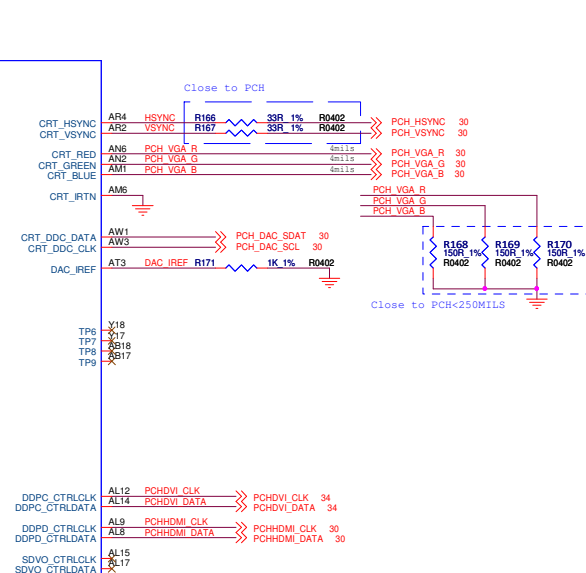
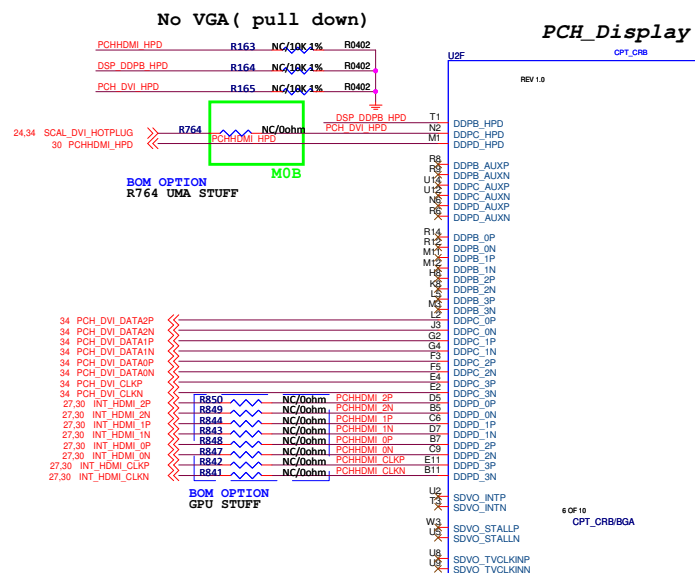


Pull HIGH for PCH

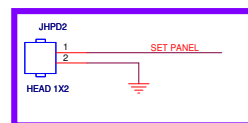
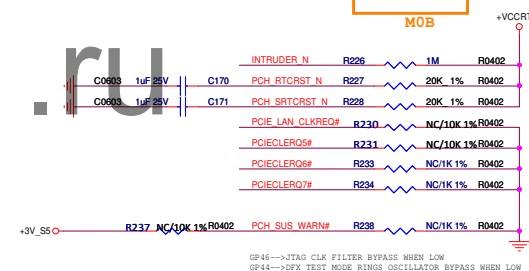


FROM CP

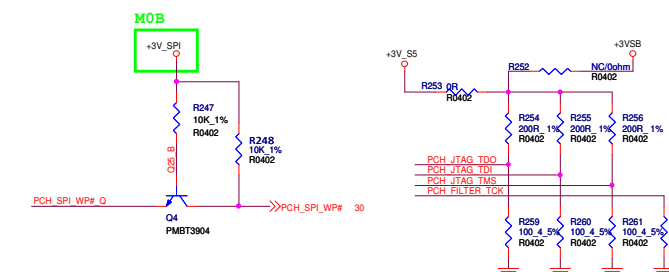
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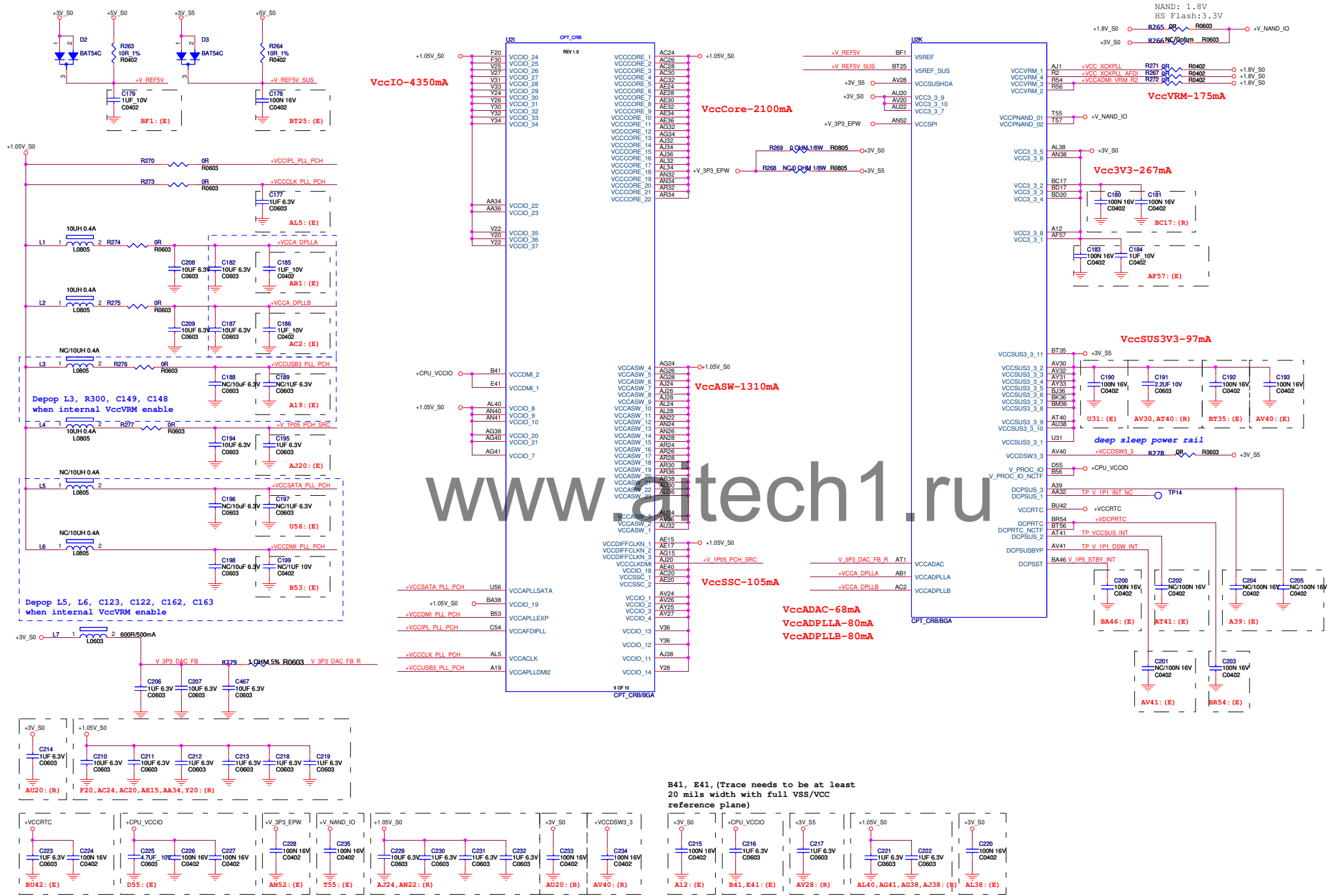
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Key Component	COVER SHEET	PCB NAME	X00000000000X	remark	<remark>
Date	Thursday, February 23, 2012	Sheet	11 of 45		



LCD SIZES	21.5"	20"
SET PANEL	HIGH	LOW



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	X02
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Date	Thursday, February 23, 2012	Sheet	12	of	45
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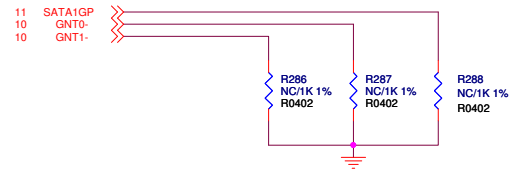


B41, E41, (Trace needs to be at least 20 mils width with full VSS/VCC reference plane)



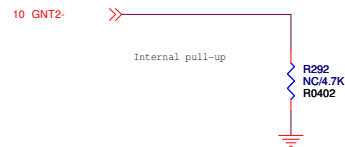
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.		T&I MODEL	C340	Rev	X02
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark	<remark>
Date	Thursday, February 23, 2012	Sheet	13 of 45		

PCH REQUIRED STRAPS

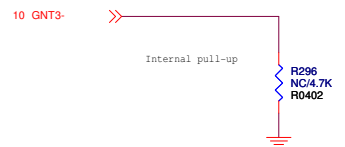


BOOT select straps

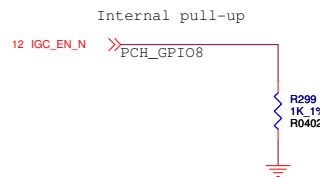
GNT1-	SATA1GP	Boot device
0	0	LPC
1	0	PCI
1	1	SPI(Default)



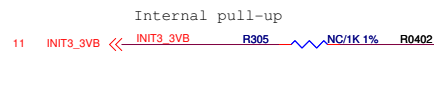
DMI AC/DC MODE
0 : AC
1 : DC *



Topblock swap override when pull-low
Signal has a weak internal pull-up

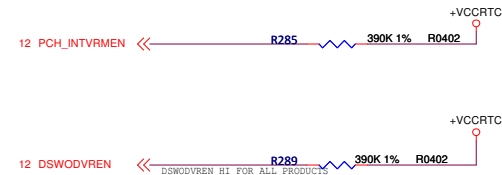


GPIO8
0 : Integrated Clocking Enable (FCIM) *
1 : Buffer Through Mode Enable (BTM)



INT3_3V#
0 : ??????????????
1 : ?????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

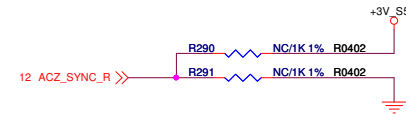


INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

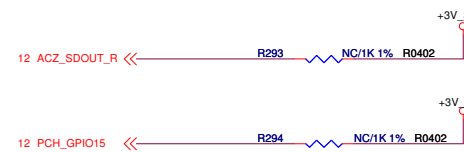
This signal enables the internal Deep Sleep 1.05 V regulators. Must be reconnected even when not supporting DSW.



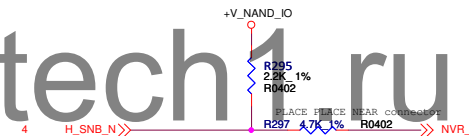
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

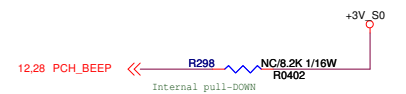
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



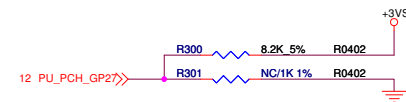
GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



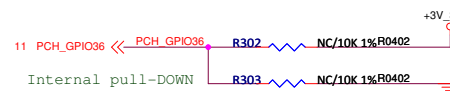
DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



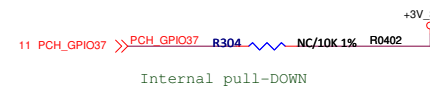
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



In Deep Sleep Power Well.
If not used, require a weak pull-up (8.2k-10k) to VccDSW3_3



Cougar point EDS PAGE:93 This signal should not be pull high



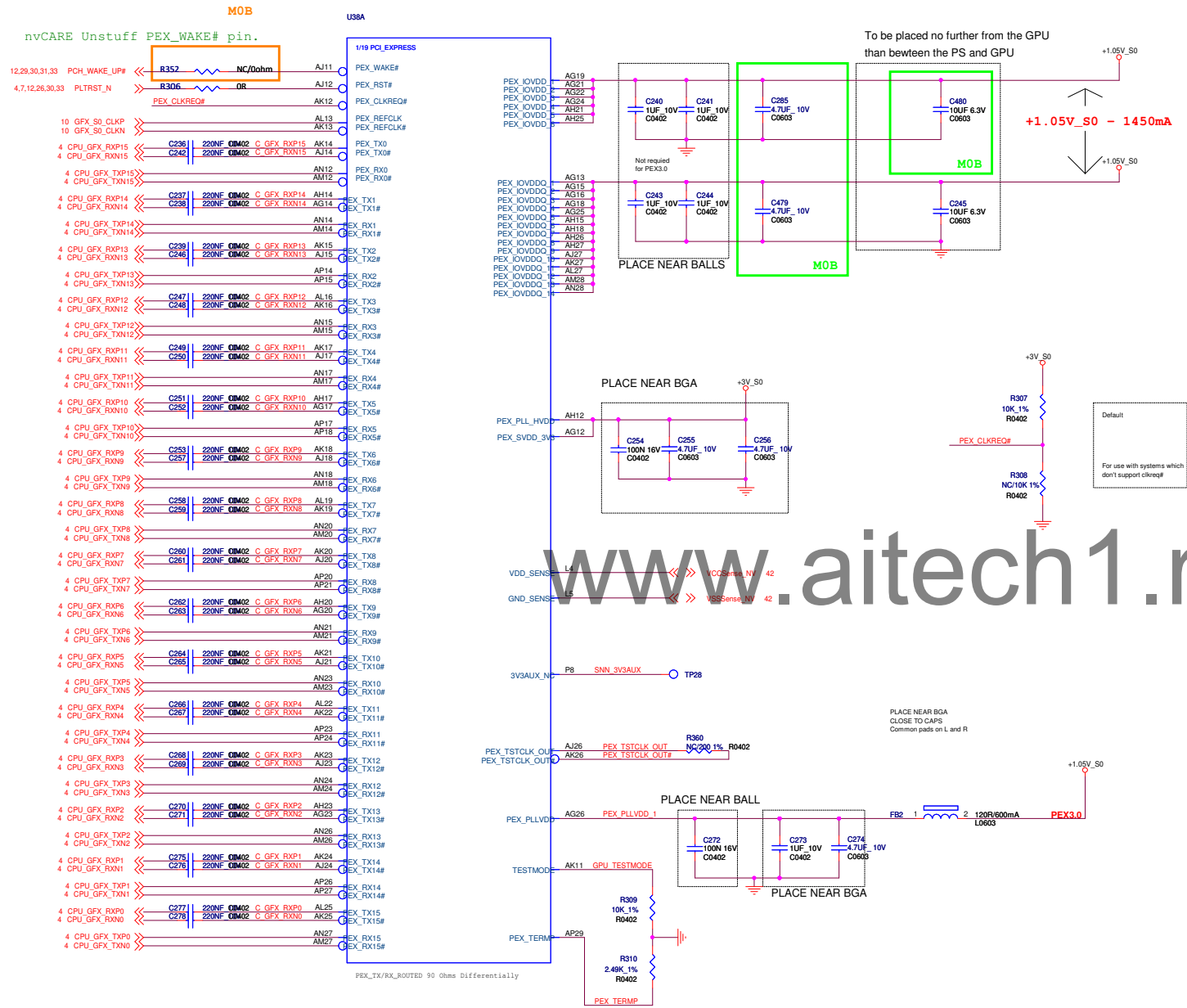
Cougar point EDS PAGE:93 This signal should not be pull high



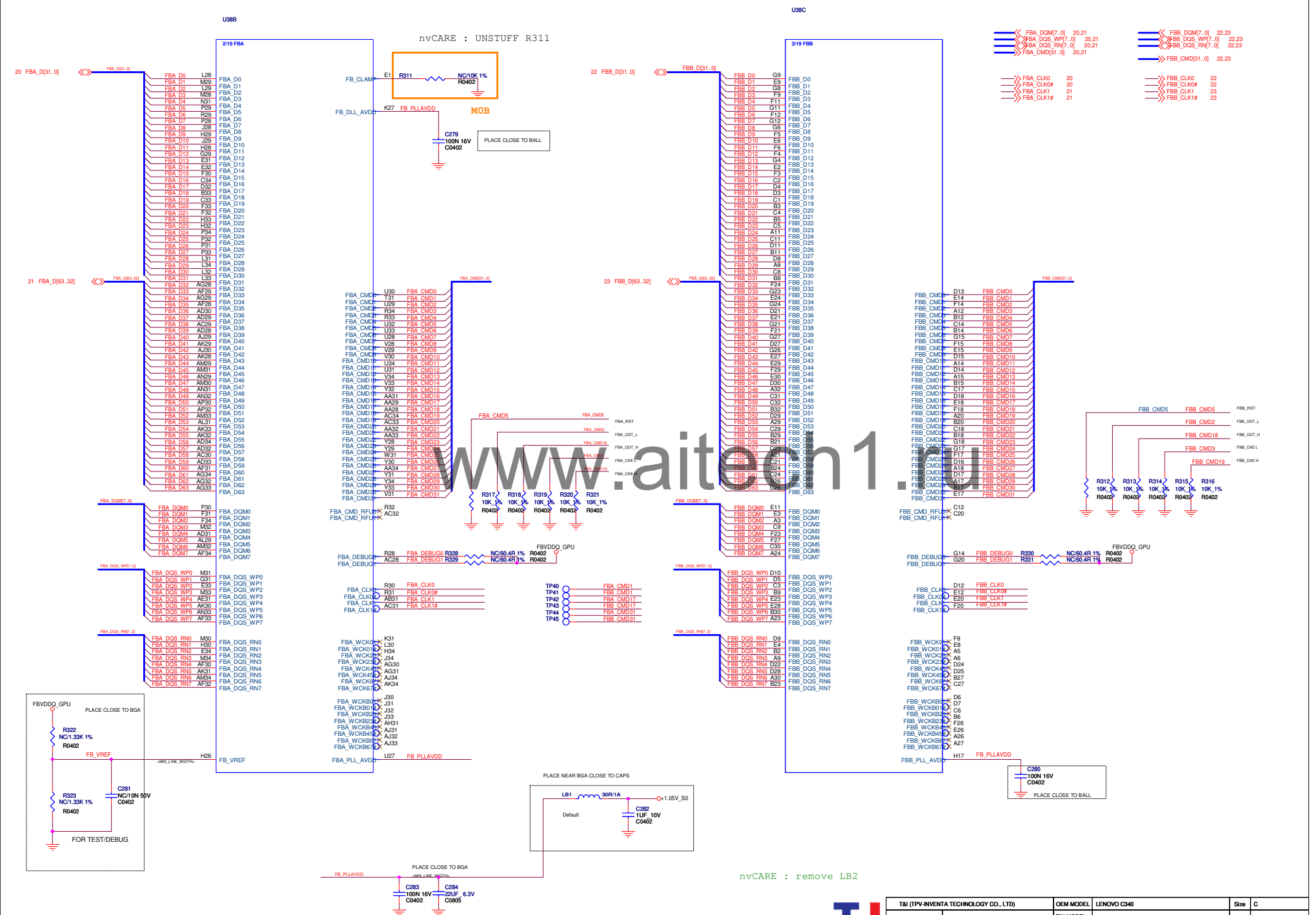
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	LENOVO C340	Size	Custom
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Thursday, February 23, 2012	Sheet	15 of 45	<remark>

PCI-Express Gen2 x16 Interface

BOM Option
UMA --> all don't stuff
GPU --> all stuff

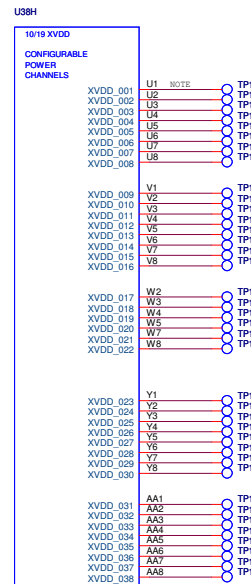
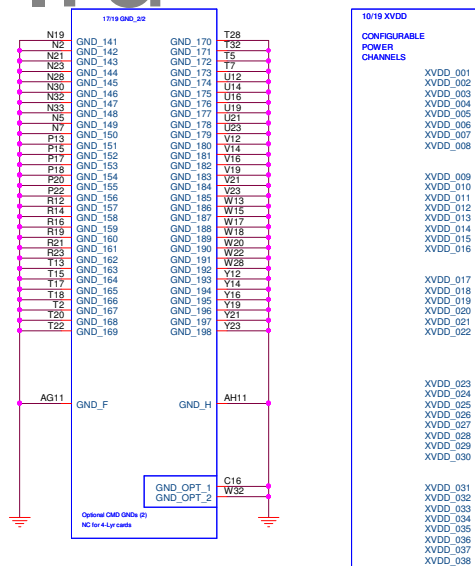
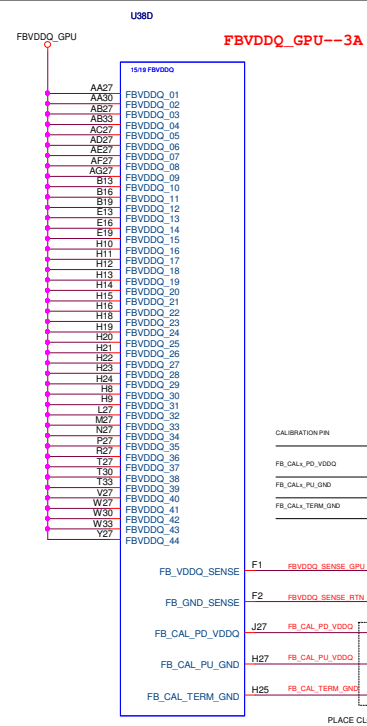
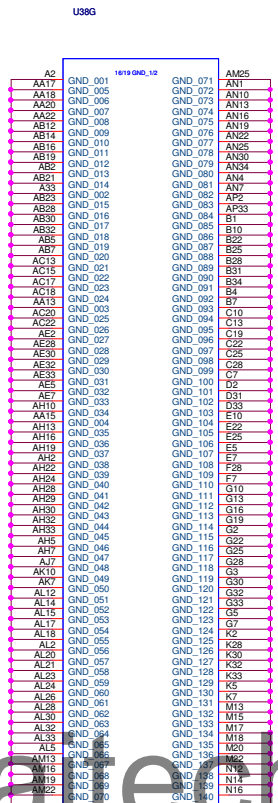
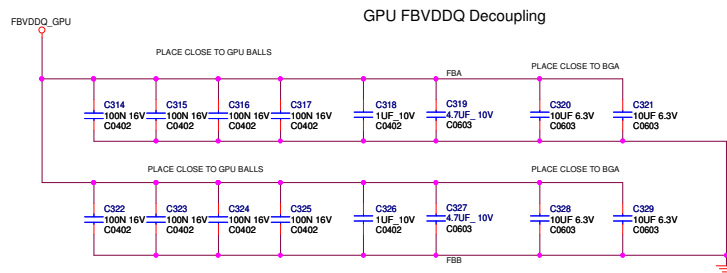
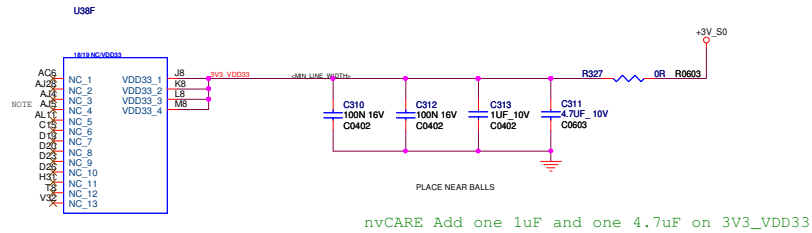
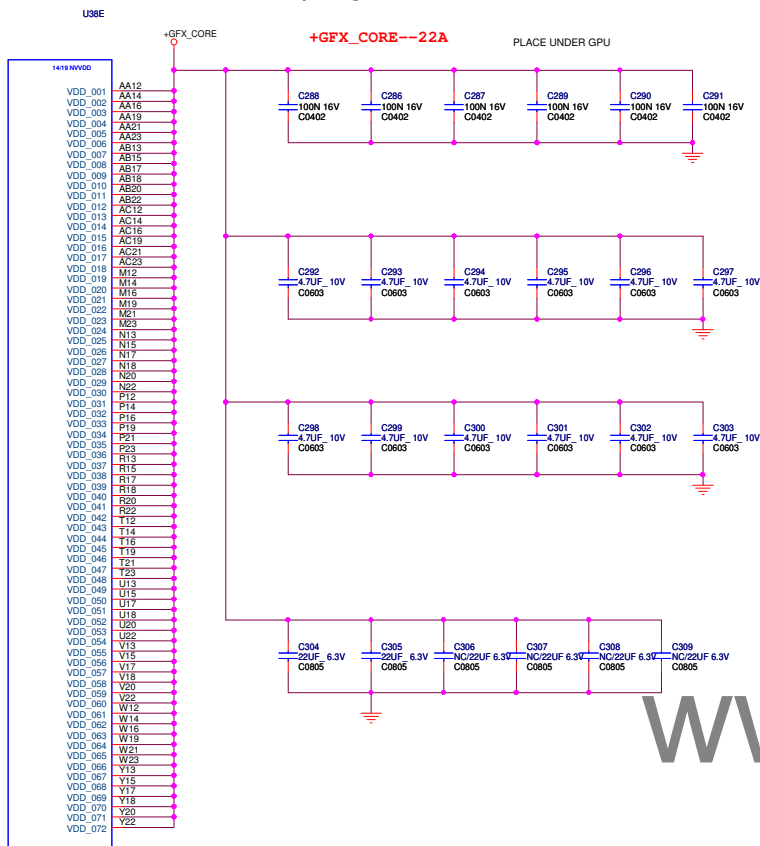


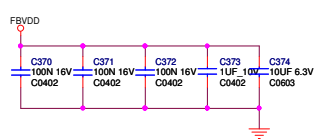
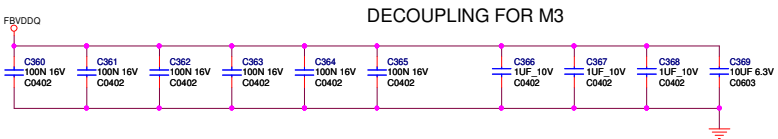
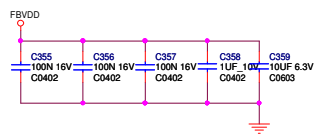
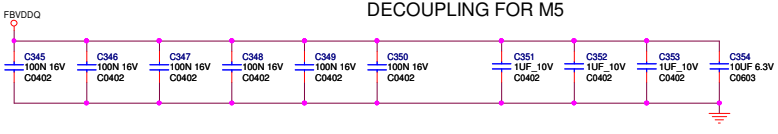
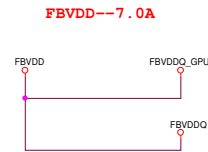
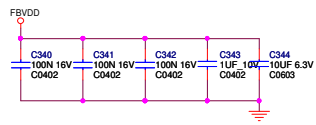
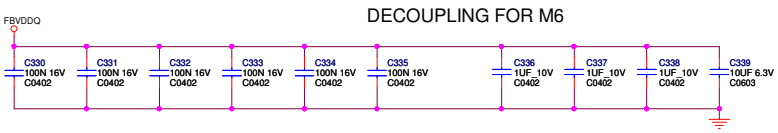
Frame Buffer Partitions A/B



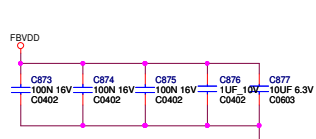
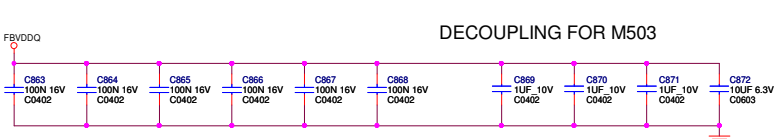
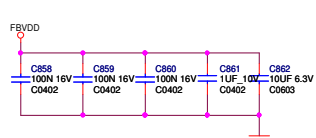
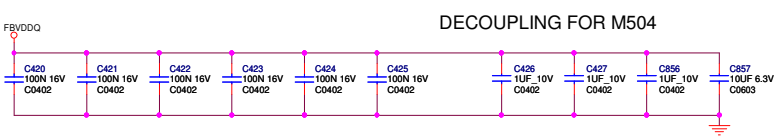
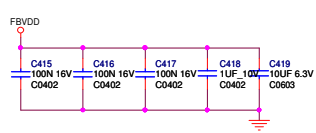
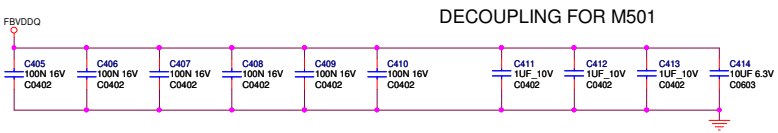
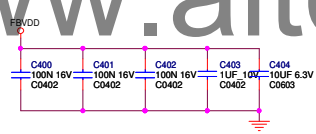
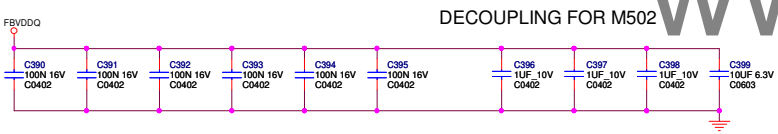
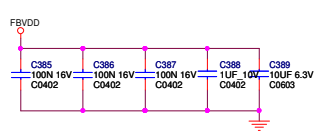
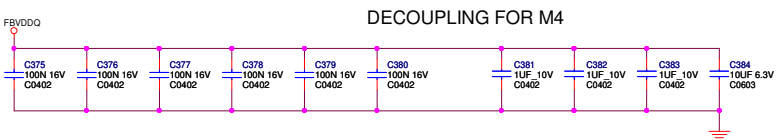
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	X02
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXXX	remark	<remark>
Date	Thursday, February 23, 2012	Sheet	17 of 45		

Power/Decoupling: NVVDD,3V3 NV,GRND,and Optional





BOM Option
UMA --> all don't stuff
GPU --> all stuff

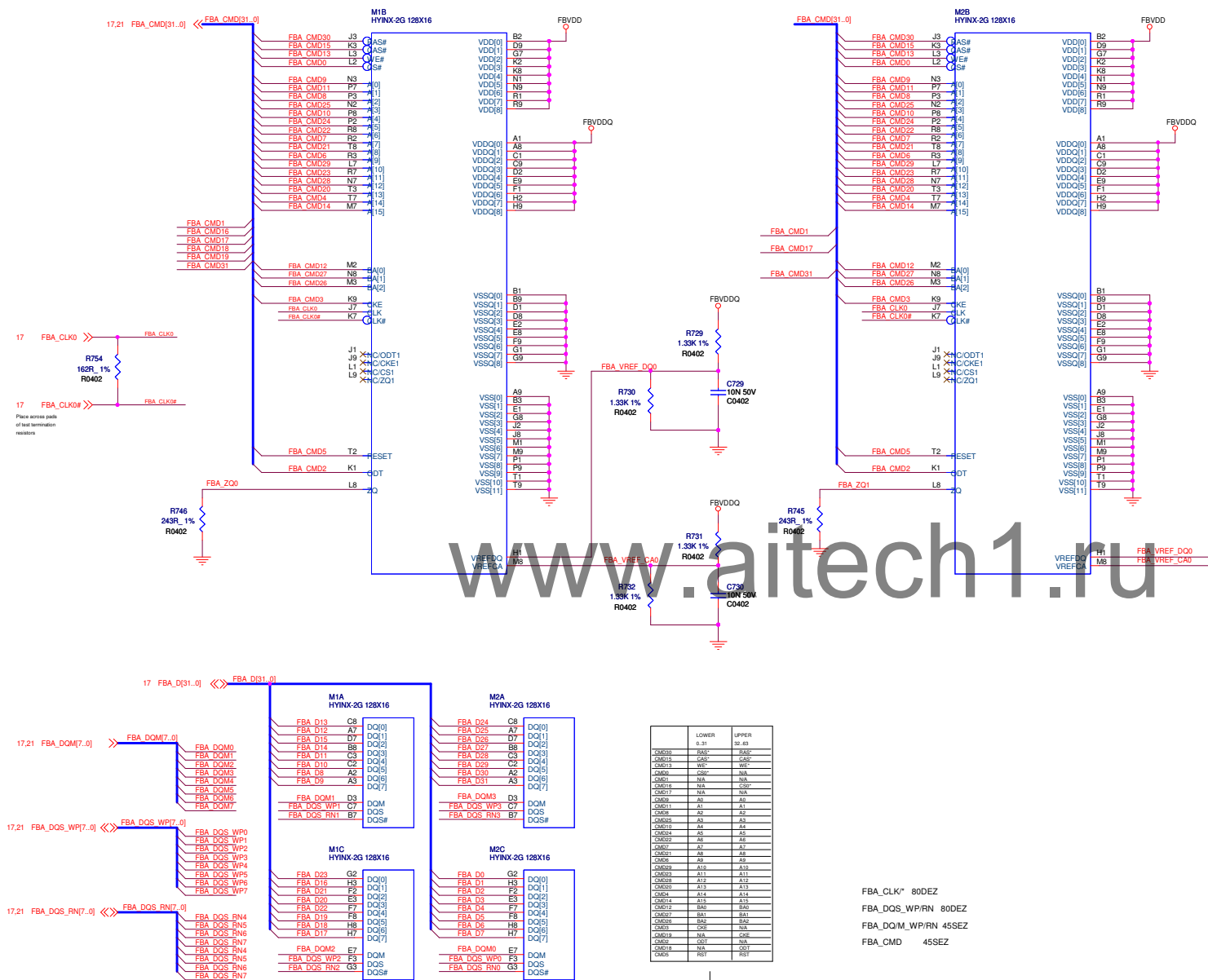


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T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Thursday, February 23, 2012	Sheet	19 of 45	

Memory Lower Partition A



BOM Option

UMA --> all don't stuff

GPU --> N13M-GE2 512MB, 64Mbx16 x4

GPU --> N13M-GE2 1GB, 128Mbx16 x4

GPU --> N13M-GE2 2GB, 128Mbx16 x8

	LOWER L-31	UPPER U-31
CM005	RAS ¹	RAS ²
CM013	RAS ¹	CAS ²
CM015	WEC ¹	WEC ²
CM060	C90 ¹	NA
CM061	NA	NA
CM062	NA	C90 ²
CM071	NA	NA
CM081	A6	A1
CM081	A1	A1
CM088	A2	A2
CM090	A2	A2
CM093	A4	A4
CM094	A5	A5
CM095	A6	A6
CM097	A7	A7
CM098	A8	A8
CM099	A10	A10
CM100	A11	A11
CM020	A12	A12
CM020	A13	A13
CM021	A14	A14
CM024	A15	A15
CM112	BA0	BA0
CM113	BA1	BA1
CM026	BA2	BA2
CM028	C0E	NA
CM029	NA	C0E
CM030	C0E	NA
CM031	NA	C0E
CM032	C0E	NA
CM033	NA	C0E
CM034	RS1	RS1

```
FBA_CLK/* 80DEZ
FBA_DQS_WP/RN 80DEZ
FBA_DQ/M_WP/RN 45SEZ
FBA_CMD 45SEZ
```

Memory Upper Partition A

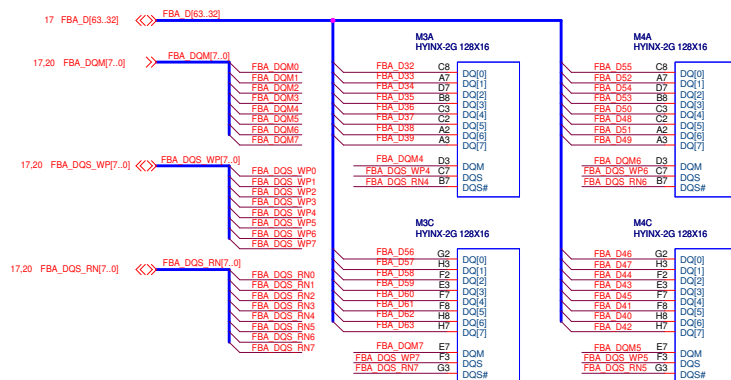
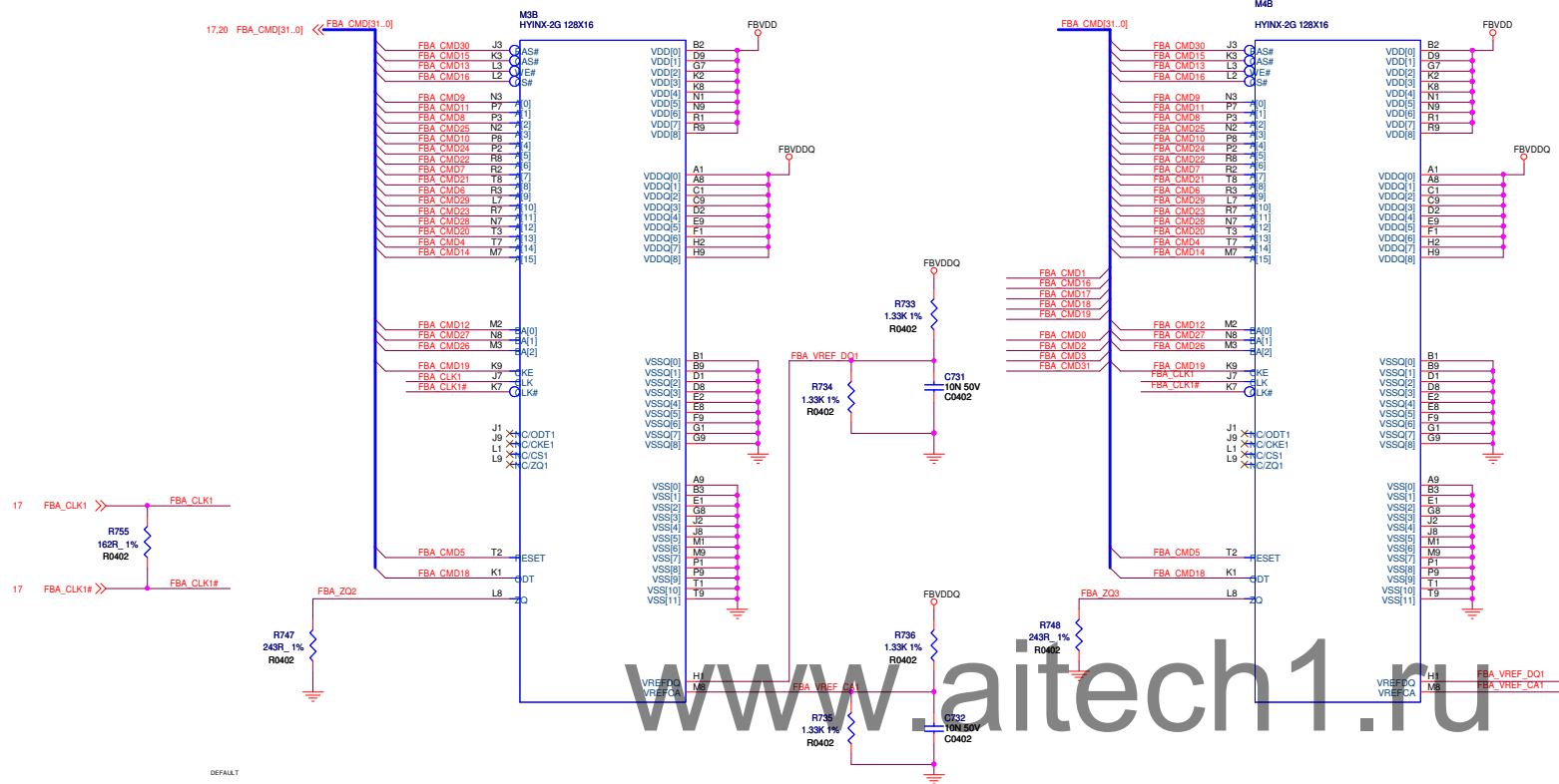
BOM Option

UMA --> all don't stuff

GPU --> N13M-GE2 512MB , 64Mbx16 x4

GPU --> N13M-GE2 1GB , 128Mbx16 x4

GPU --> N13M-GE2 2GB , 128Mbx16 x8

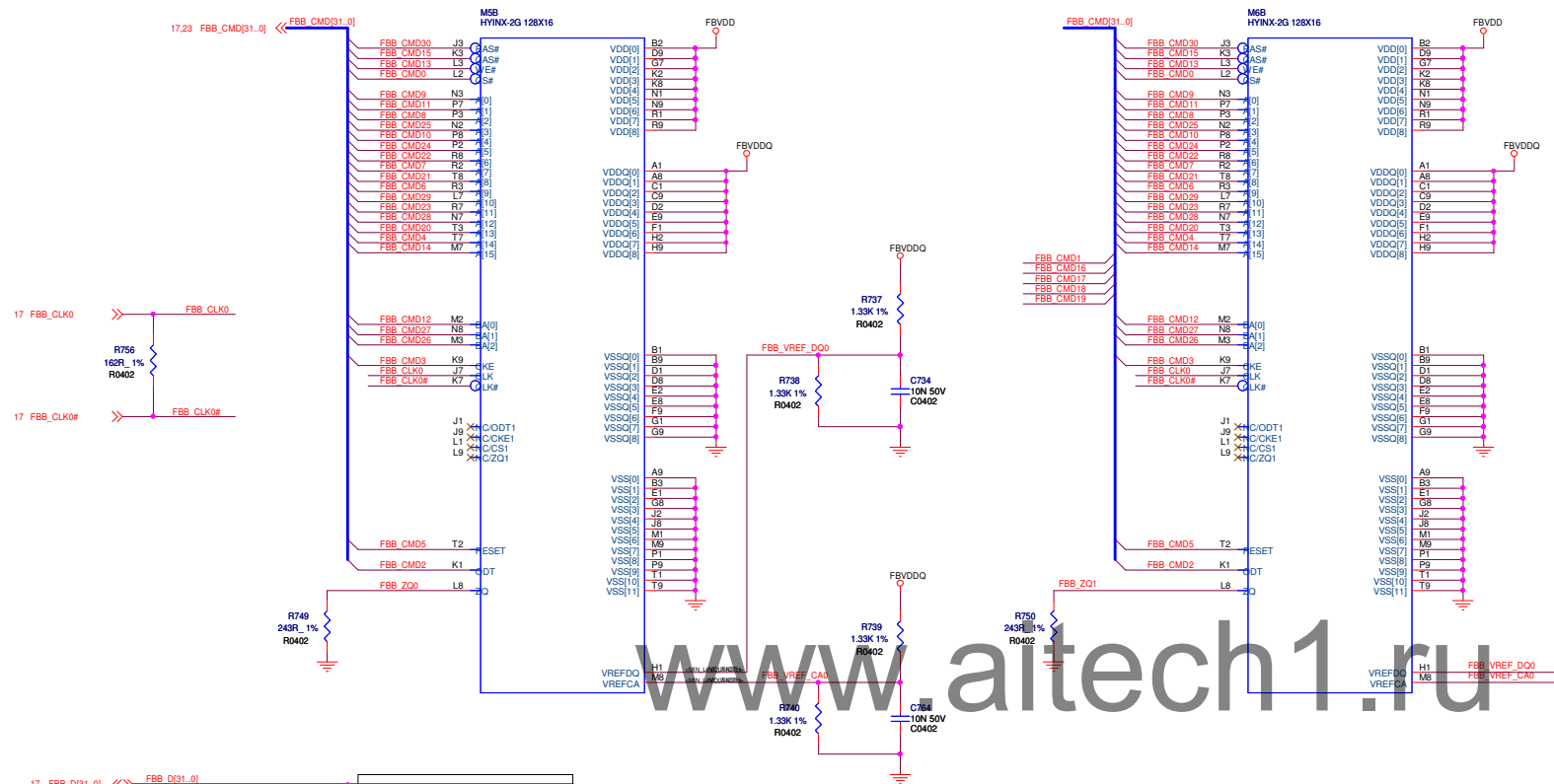


	LOWER	UPPER
	0.31	32.40
CM005	WAS	WAS
CM006	CAS	CAS
CM013	WE	WE
CM014	CSE	N/A
CM031	N/A	N/A
CM032	N/A	N/A
CM039	A0	A0
CM041	A1	A1
CM048	A2	A2
CM053	A3	A3
CM055	A4	A4
CM054	A5	A5
CM056	A6	A6
CM057	A7	A7
CM058	A8	A8
CM059	A9	A9
CM069	A10	A10
CM072	A11	A11
CM073	A12	A12
CM080	A13	A13
CM081	A14	A14
CM084	A15	A15
CM087	BAD	BAD
CM092	BA1	BA1
CM098	BAD	BAD
CM103	CSE	N/A
CM109	N/A	CSE
CM122	ODT	N/A
CM125	N/A	ODT
CM126	RO1	RO1

IN USE ON
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T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	X02
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX		
Date	Thursday, February 29, 2012	Sheet	1 of 45	remark	<remark>

Memory Lower Partition B



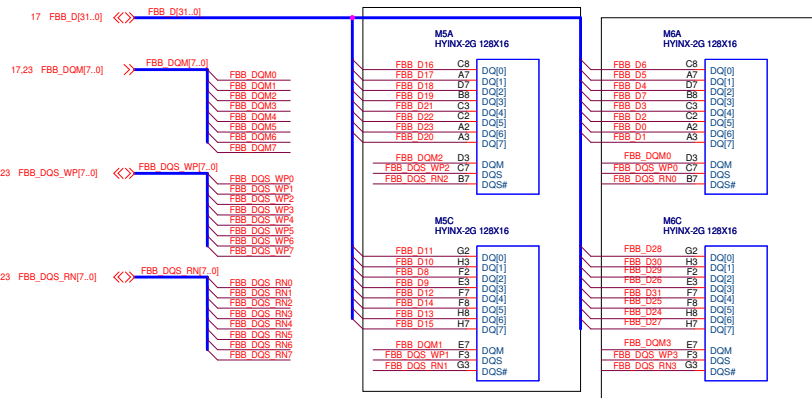
BOM Option

UMA --> all don't stuff

GPU --> N13M-GE2 512MB, 64Mbx16 x4

GPU --> N13M-GE2 1GB , 128Mbx16 x4

GPU --> N13M-GE2 2GB , 128Mbx16 x8



SWAP PIN

	LOWER	UPPER
	8.31	32.83
CMD0	CAS0	CAS0
CMD05	CAS0	CAS0
CMD13	WE0	WE0
CMD14	CSP0	CSP0
CMD1	N/A	N/A
CMD2	N/A	CSP0
CMD3	N/A	CSP0
CMD9	A0	A0
CMD10	A1	A1
CMD8	A2	A2
CMD20	A3	A3
CMD15	A4	A4
CMD24	A5	A5
CMD25	A6	A6
CMD17	A7	A7
CMD21	A8	A8
CMD19	B0	B0
CMD29	A10	A10
CMD22	A12	A12
CMD23	A13	A13
CMD24	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD11	BA1	BA1
CMD28	BA2	BA2
CMD9	C0E	N/A
CMD19	N/A	C0E
CMD2	C0T	N/A
CMD19	N/A	C0T
CMD5	POST	POST

IN USE ON
THIS PAGE

FBA_CLK/* 80DEZ

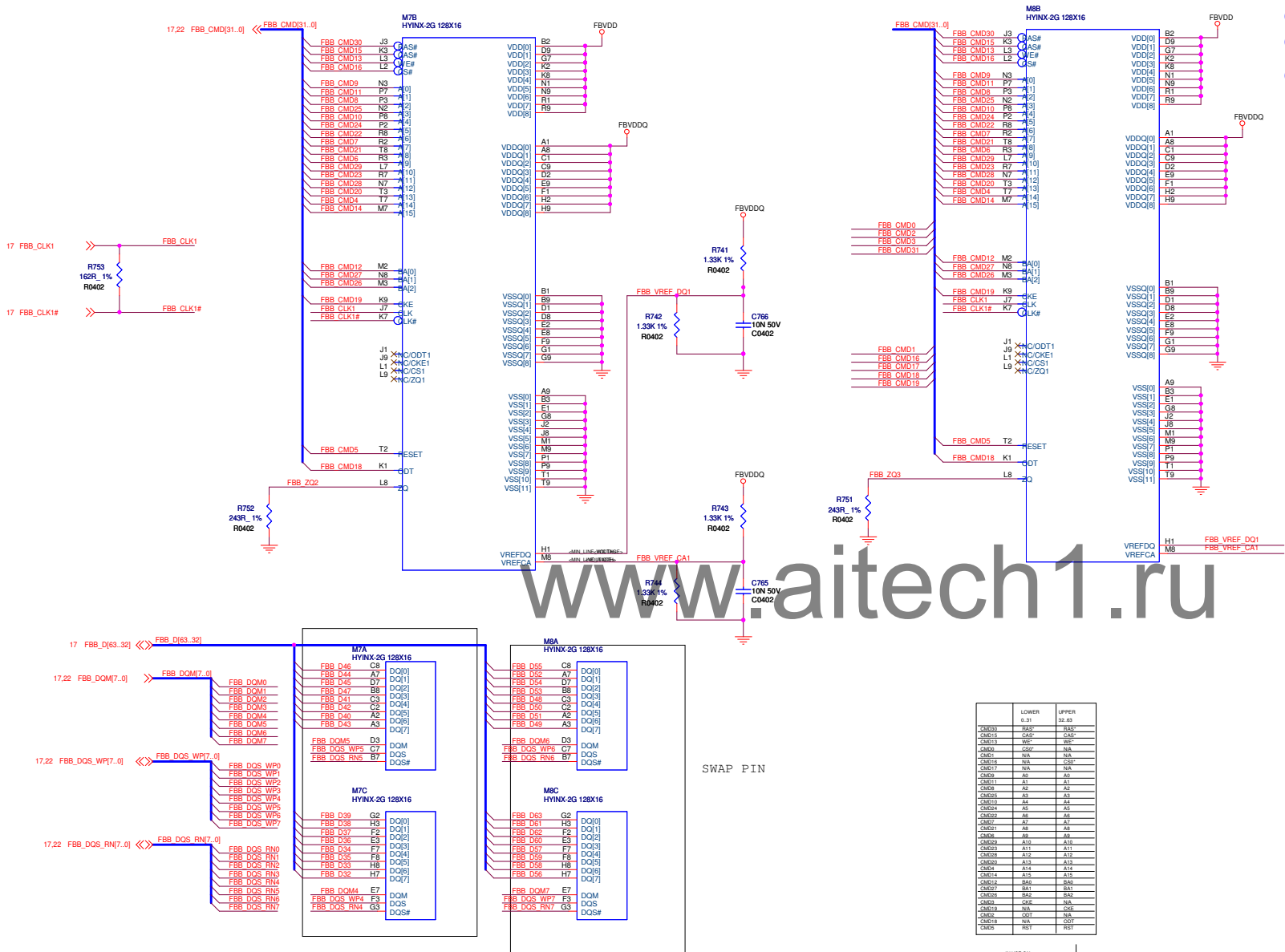
FBA_DQS_WP/RN 80DEZ

FBA_DQ/M_WP/RN 45SEZ

FBA_CMD 45SEZ

T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	X02
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXXXX	remark	<remark>
Date	Thursday, February 23, 2012	Sheet	22 of 45		

Memory Upper Partition B



BOM Option
UMA --> all don't stuff
GPU --> N13M-GE2 512MB, 64Mbx16 x4
GPU --> N13M-GE2 1GB, 128Mbx16 x4
GPU --> N13M-GE2 2GB, 128Mbx16 x8

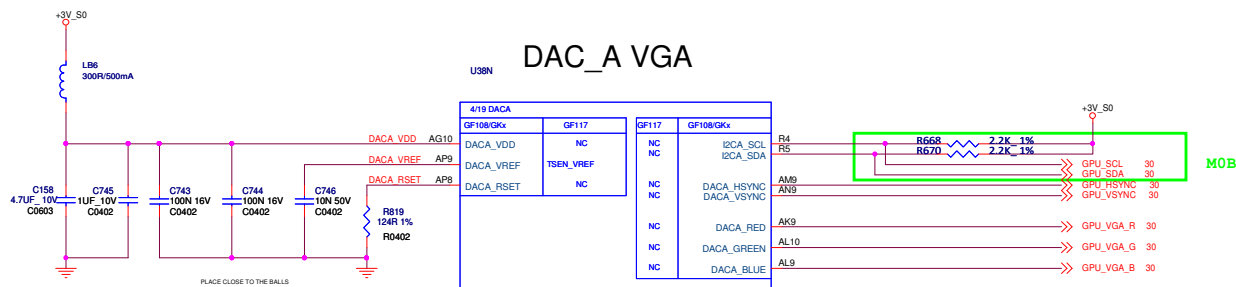
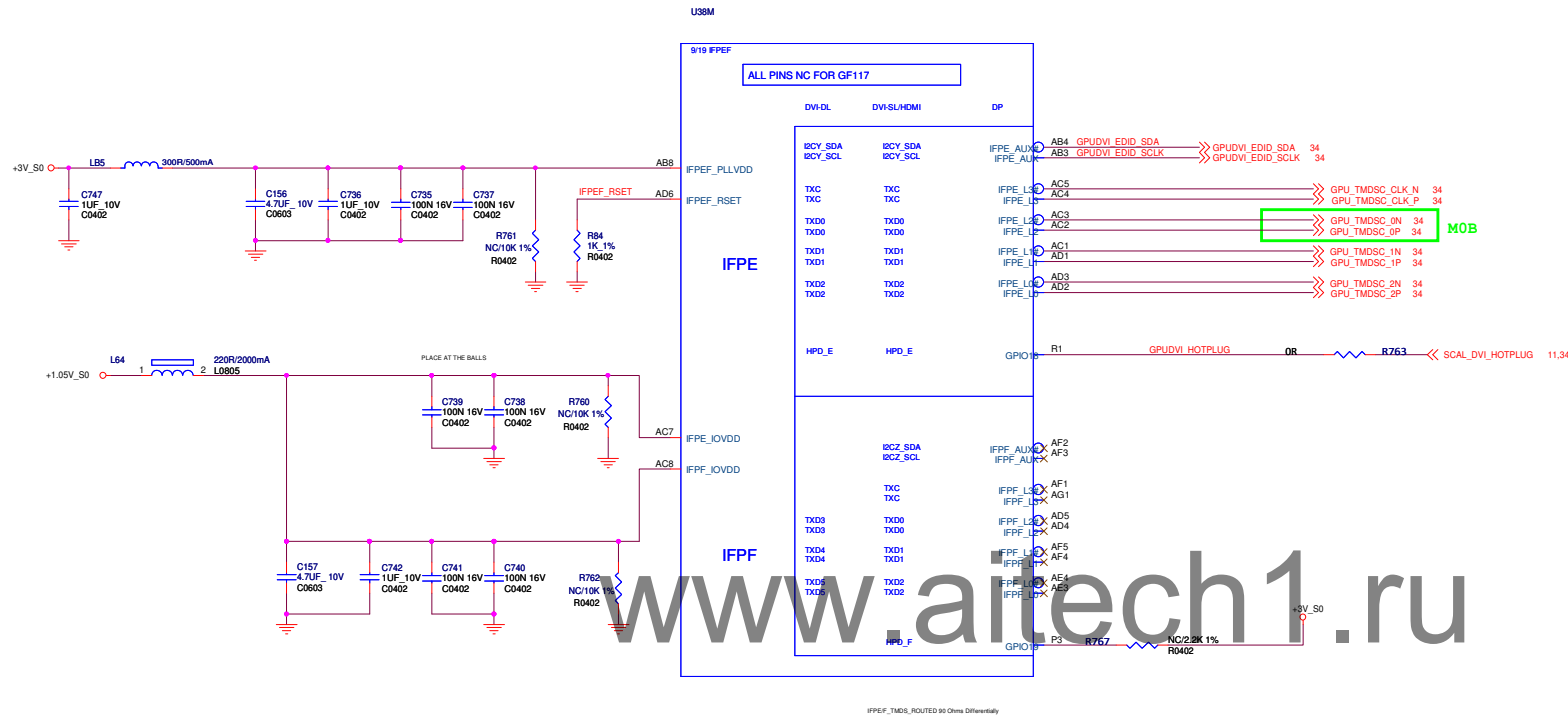
	LOWER 8-31	UPPER 32-63
Q4000	BA0P	BA0P
Q4001	BA0P	BA0P
Q4002	BA0P	BA0P
Q4003	BA0P	BA0P
Q4004	BA0P	BA0P
Q4005	BA0P	BA0P
Q4006	BA0P	BA0P
Q4007	BA0P	BA0P
Q4008	BA0P	BA0P
Q4009	BA0P	BA0P
Q4010	BA0P	BA0P
Q4011	BA0P	BA0P
Q4012	BA0P	BA0P
Q4013	BA0P	BA0P
Q4014	BA0P	BA0P
Q4015	BA0P	BA0P
Q4016	BA0P	BA0P
Q4017	BA0P	BA0P
Q4018	BA0P	BA0P
Q4019	BA0P	BA0P
Q4020	BA0P	BA0P
Q4021	BA0P	BA0P
Q4022	BA0P	BA0P
Q4023	BA0P	BA0P
Q4024	BA0P	BA0P
Q4025	BA0P	BA0P
Q4026	BA0P	BA0P
Q4027	BA0P	BA0P
Q4028	BA0P	BA0P
Q4029	BA0P	BA0P
Q4030	BA0P	BA0P
Q4031	BA0P	BA0P
Q4032	BA0P	BA0P
Q4033	BA0P	BA0P
Q4034	BA0P	BA0P
Q4035	BA0P	BA0P
Q4036	BA0P	BA0P
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Q4038	BA0P	BA0P
Q4039	BA0P	BA0P
Q4040	BA0P	BA0P
Q4041	BA0P	BA0P
Q4042	BA0P	BA0P
Q4043	BA0P	BA0P
Q4044	BA0P	BA0P
Q4045	BA0P	BA0P
Q4046	BA0P	BA0P
Q4047	BA0P	BA0P
Q4048	BA0P	BA0P
Q4049	BA0P	BA0P
Q4050	BA0P	BA0P

INUSE ON
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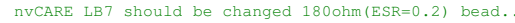


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	LENOWO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev
Key Component	COVER SHEET	POB NAME	XXXXXXXXXXXX	remark
Date	Thursday, February 23, 2012	Sheet	23 of 45	

IFPE/F Dual Link TMDS DVI-I



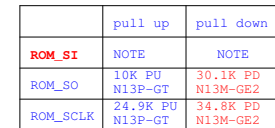
The circuit diagram shows the connection of the ROM CS# pin to the U30S10EVSNIG microcontroller. The ROM CS# pin is connected to the VCC pin of the microcontroller through a pull-up resistor R770 (10K_1% R0402). The microcontroller's VCC pin is connected to the positive supply rail. The microcontroller's GND pin is connected to the ground rail. The microcontroller's Q1D pin is connected to the positive supply rail through a resistor R825 (NC4.99K 1%-04 R0402). The microcontroller's Q1S pin is connected to the ground rail through a resistor R826 (NC4.99K 1%-04 R0402).



	FU_3V3	PD_GND
4.99K	1000 (8)	0000 (0)
10.0K	1001 (9)	0001 (1)
15.0K	1010 (A)	0010 (2)
20.0K	1011 (B)	0011 (3)
24.9K	1100 (C)	0100 (4)
30.1K	1101 (D)	0101 (5)
34.8K	1110 (E)	0110 (6)
45.3K	1111 (F)	0111 (7)

```
NOTE N13M-GE2
128X16 DDR3 samsung UX7 K4W2G1646C-HC11
PD 45.3K STRAP CODE 07(0111)
64X16 DDR3 samsung UX3 K4W1G1646G-BC11
PD 20K STRAP CODE 03(0011)

128X16 DDR3 Hynix UX6 H5TQ2G63BFR-11C
PD 34.8K Hynix UX6 H5TQ2G63DFR-11C
PD 34.8K STRAP CODE 06(0110)
64x16 DDR3 Hynix UX2 H5TQ1G63DFR-11C
PD 15K STRAP CODE 02(0010)
```



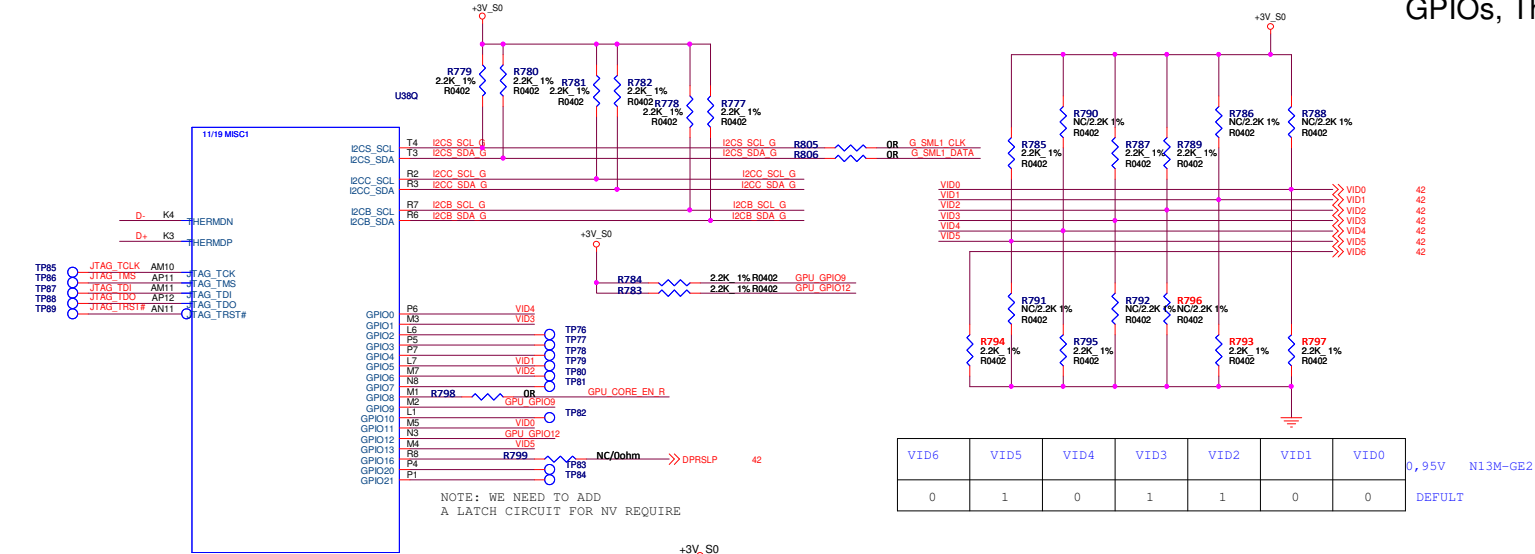
6013A0107901	45S_K_4_1%	+	6019B0906601	SS	K4W2G1646C-HC11
6113A0003601	20K_K_4_1%	+	6019B0818501	SS	K4W1G1646G-BC11
6013A0017901	34.8K_K_4_1%	+	6019B0938301	Hynix	H5TQ2G63DFR-11C
6013A0017201	15K_K_4_1%	+	6019B0873101	Hynix	H5TQ1G63DFR-11C

GF108 STRAPPING MODE TABLE			
PIN NAME	MULTI-LEVEL	BINARY PRODUCTION	BINARY BRINGUP
MULTI_STRAP_REF_GND	40.2K TO GND	NO STUFF	NOT SUPPORTED

GF117/GK10X STRAPPING MODE TABLE			
PIN NAME	MULTI-LEVEL	BINARY PRODUCTION	BINARY BRINGUP
MULTI_STRAP_REF_GND	40.2K TO GND	NOT SUPPORTED	NO STUFF

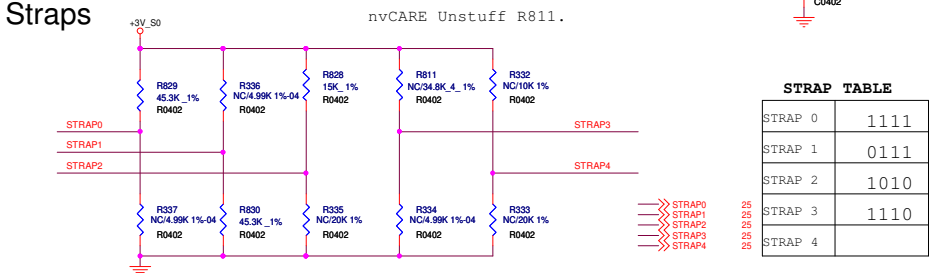
GPIOs, Thermal Sensor, I2C/GPIO Expanders

GPIO	Function	GPIO	Function
GPIO 0	Debug/Service Header/Alt_Fan PWM		I2C PORT C
GPIO 1	VID 2	EXPND 0	Level Shifter Error Correction
GPIO 2	LCD brightness control (BL PWM)	EXPND 1	NVGEM GPIO EXP1/ PS_Margin*
GPIO 3	LCD Power enable (PPEN)	EXPND 2	NVGEM GPIO EXP2/PS_MR*
GPIO 4	LCD Backlight enable (BLEN)	EXPND 3	GPIO_DEBUG_SERVICE HEADER
GPIO 5	VID 0		
GPIO 6	VID 1		
GPIO 7	3D STEREO		SMBUS
GPIO 8	GPU Overtemp	EXPND 4	GPU_PS_EN
GPIO 9	GPU thermal Alert	EXPND 5	RSVD
GPIO 10	FB Vref Control (not used sDDR3)	EXPND 6	PEX_RST
GPIO 11	FBVDD/Q VID (Reserved)	EXPND 7	RSVD
GPIO 12	PWR_Level AC Detect		
GPIO 13	PS1 Vprgm Enable		
GPIO 14	HPD for IFP AB (not used)		
GPIO 15	HPD for IFP C (HDMI/DP)		
GPIO 16	Fan PWM control		
GPIO 17	HPD for IFP D (DP)		
GPIO 18	HPD for IFP E (DVI-I DL)		
GPIO 19	HPD for IFP F (not used)		
GPIO 20	NVGEM Debug GPIO13		
GPIO 21	NVGEM Debug GPIO14		



	pull up	pull down
STARP0	GR133 PU 45.3K	
STARP1		GR139 PD 34.8K
STARP2	GR135 15K PU N13M-GE2	GR140 10K PD N13P-GT
STARP3	GR136 PU 34.8K 1110	
STARP4		GR142 PD GR142 NC N13P-GT N13M-GE2

Straps



STRAP TABLE

STRAP 0	1111
STRAP 1	0111
STRAP 2	1010
STRAP 3	1110
STRAP 4	

RESISTER MAPING

	PU_3V3	PD_GND
4.99K	1000	0000
10.0K	1001	0001
15.0K	1010	0010
20.0K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

GF108 STRAP PIN MODE TABLE

PIN NAME	MULTI-LEVEL bit [3:0]	BINARY PRODUCTION	BINARY BRINGUP
STRAP0	USER[3:0]	RAMCFG0	
STRAP1	3GIO_PADCFG_ADR[3:0]	RAMCFG1	
STRAP2	PCI_DEVID[3:0]	RAMCFG2	
ROM_SCLK	PCIDEVID[4], SUB_VENDOR, SLOT_CLK, PEX_PLL_EN_TERM	PCI_DEVID3	
ROM_SI	RAMCFG[3:0]	PCI_DEVID_EXT	
ROM_SO	XCLK_417, FB0_BAR_SIZE, SMB_ALT_ADDR, VGA_DEVICE	XCLK_417	

NOTE 2: See table 1 for the correct value/location of the strap resistor for the desired modes

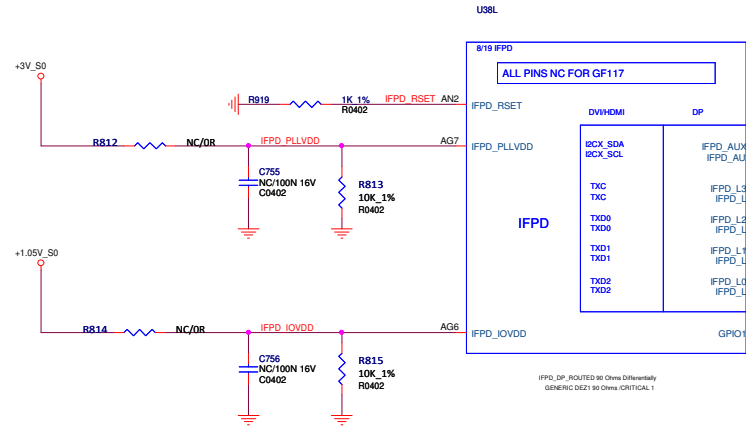
NOTE 3: Bring-up SKU(s) have jumper configurable subvendor and DEVID_4 settings see the ROM_SCLK STRAP

T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Thursday, February 23, 2012	Sheet	26 of 45	

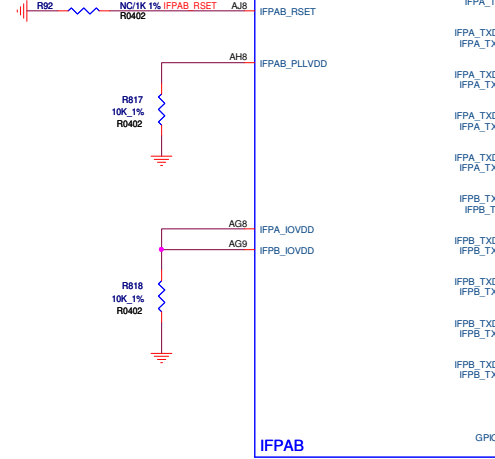


IFPA/B LVDS Dual Link

nvCARE : IFPD no used, 10K PD at IFPD_PLLVDD and IFPD_IOVDD.

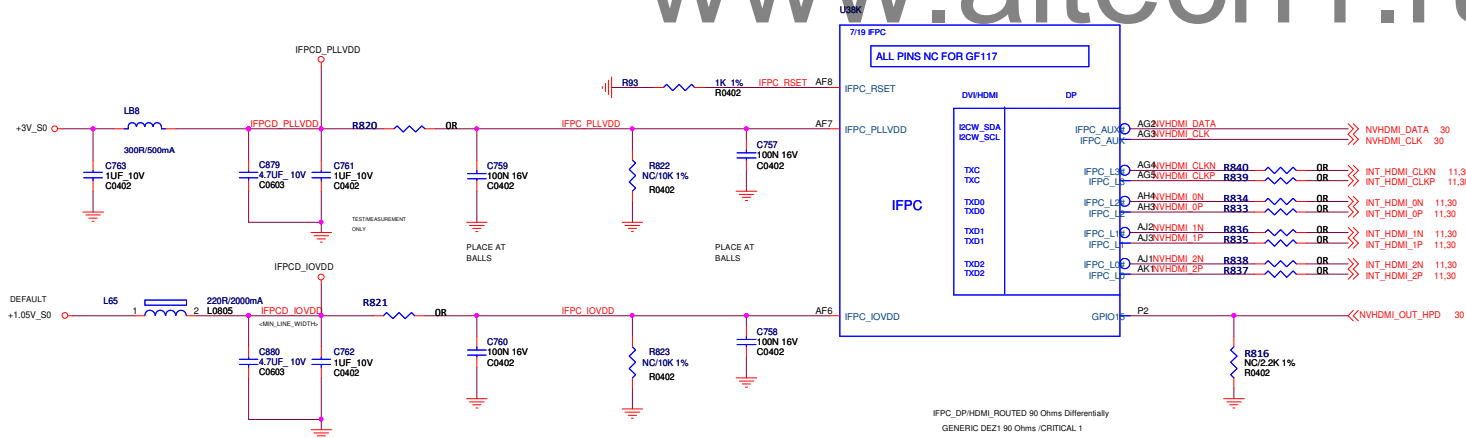


IFPAB ONLY: NO STUFF RESET is used
Required when external reference is used



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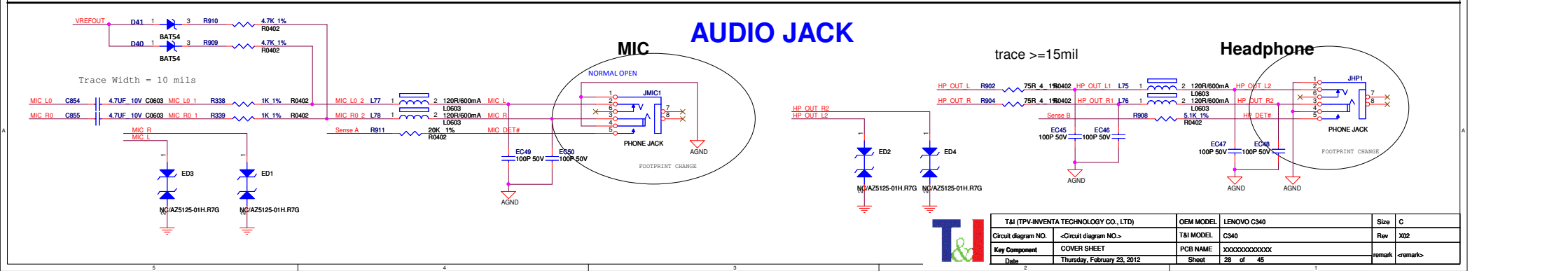
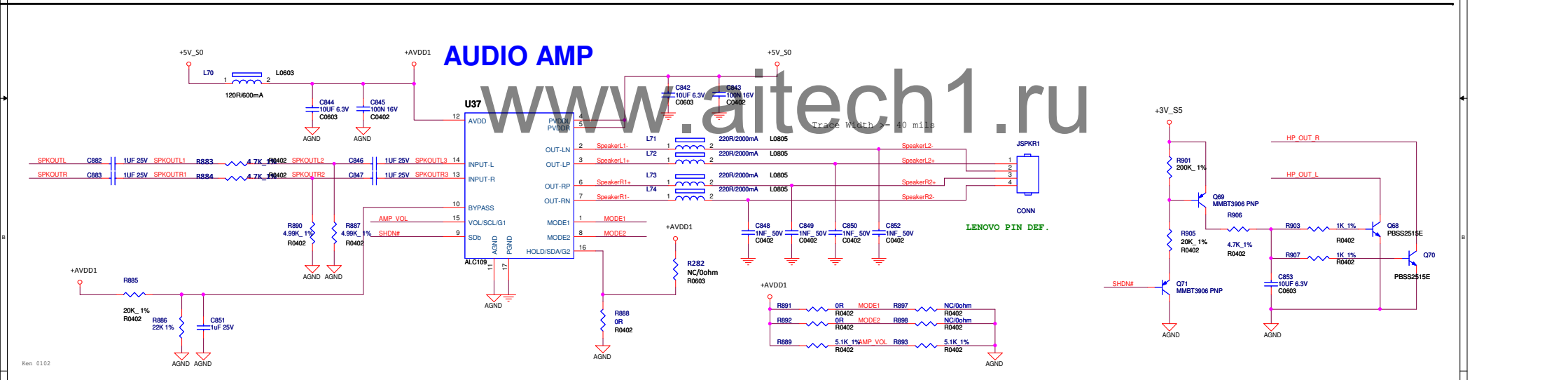
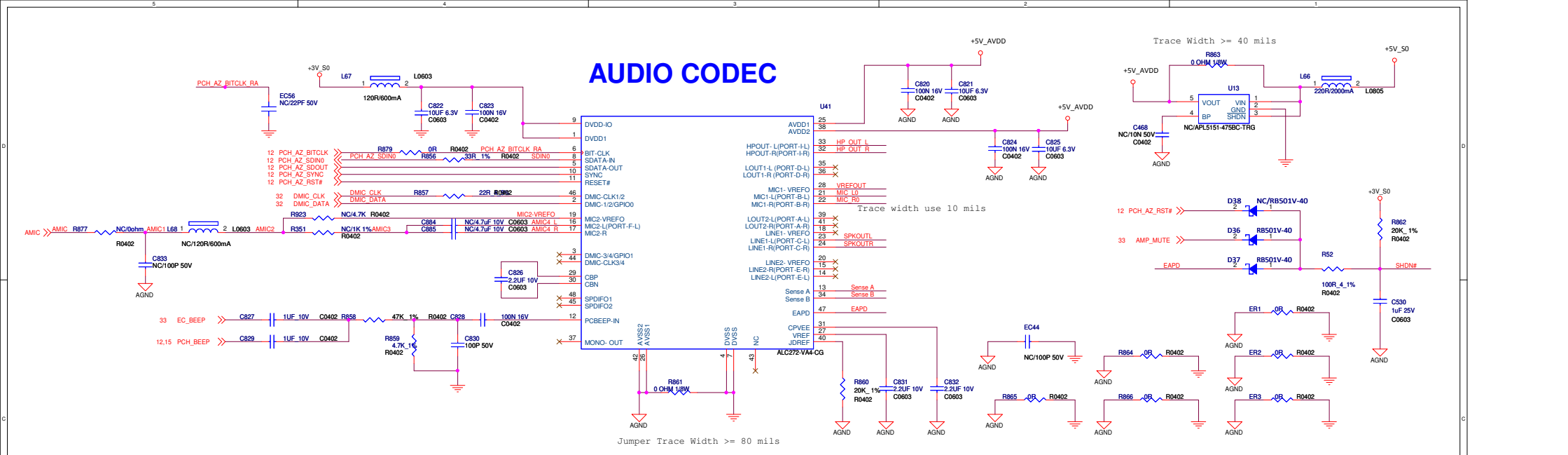
IFPC NATIVE HDMI OR DP



IFPC_DP/HDMI_ROUTED 90 Ohms Differentially
GENERIC DE21 90 Ohms /CRITICAL 1

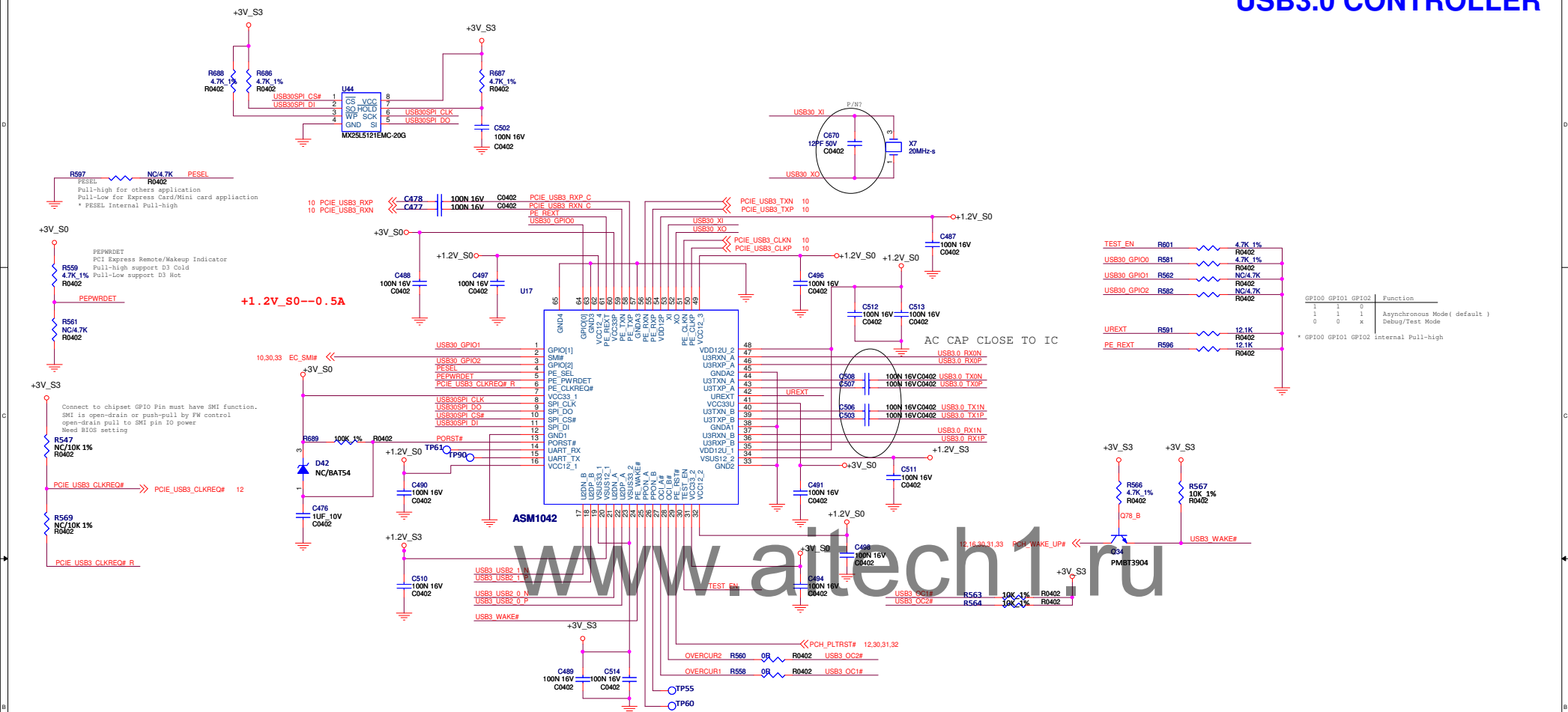


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Thursday, February 23, 2012	Sheet	27 of 45	

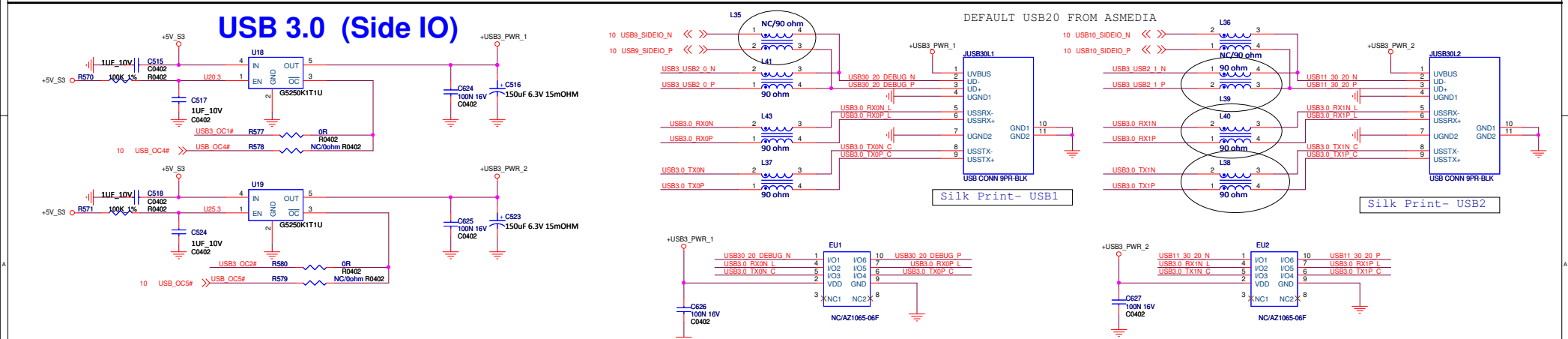


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Thursday, February 23, 2012	Sheet	28 of 45	<remark>

USB3.0 CONTROLLER



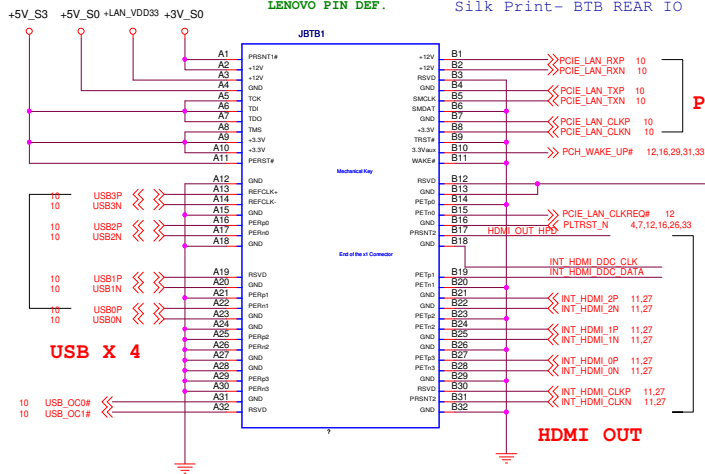
USB 3.0 (Side IO)



REAR I/O

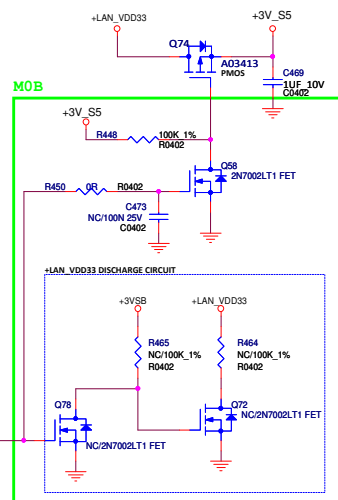
LENOVO PIN DEF.

Silk Print- BTB REAR IO

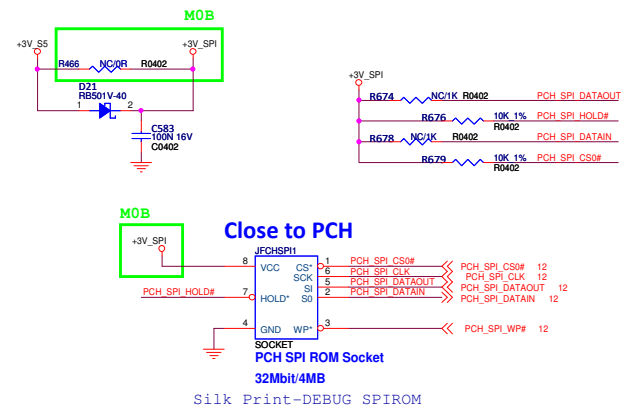


PCIE LAN

HDMI OUT



PCH SPI ROM



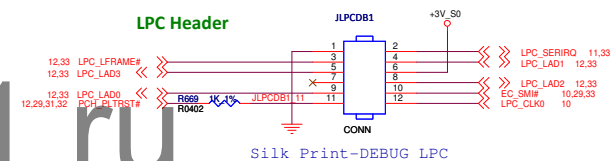
Close to PCH

PCH SPI ROM Socket

Silk Print-DEBUG SPIROM

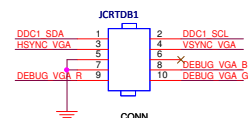
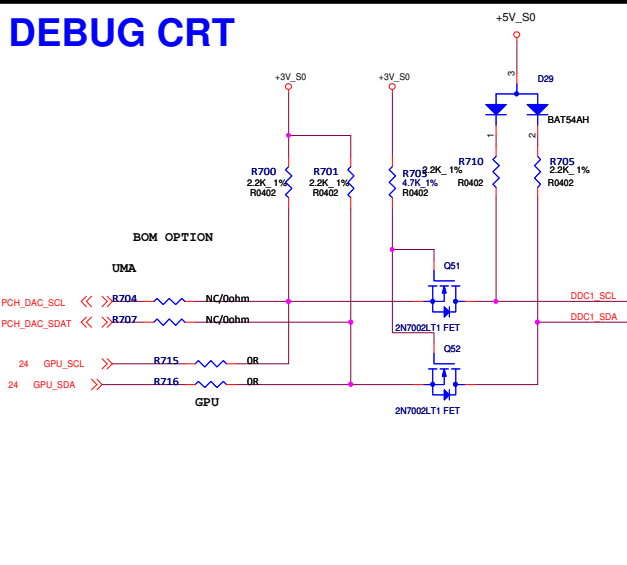
LPC DEBUG PORT

LPC Header

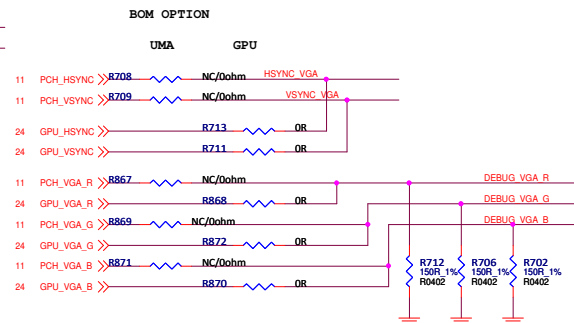


Silk Print-DEBUG LPC

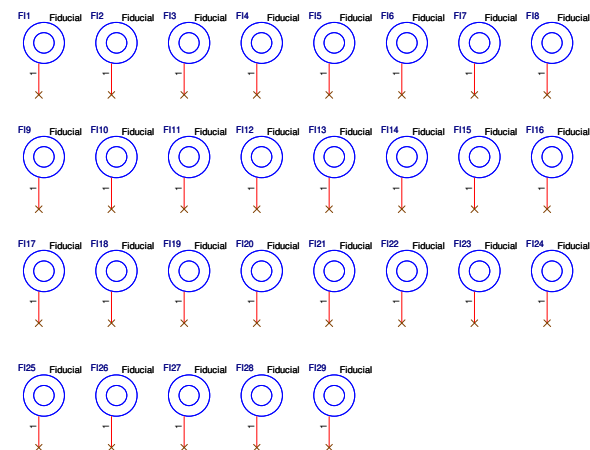
DEBUG CRT



Silk Print-DEBUG CRT



Optical Point



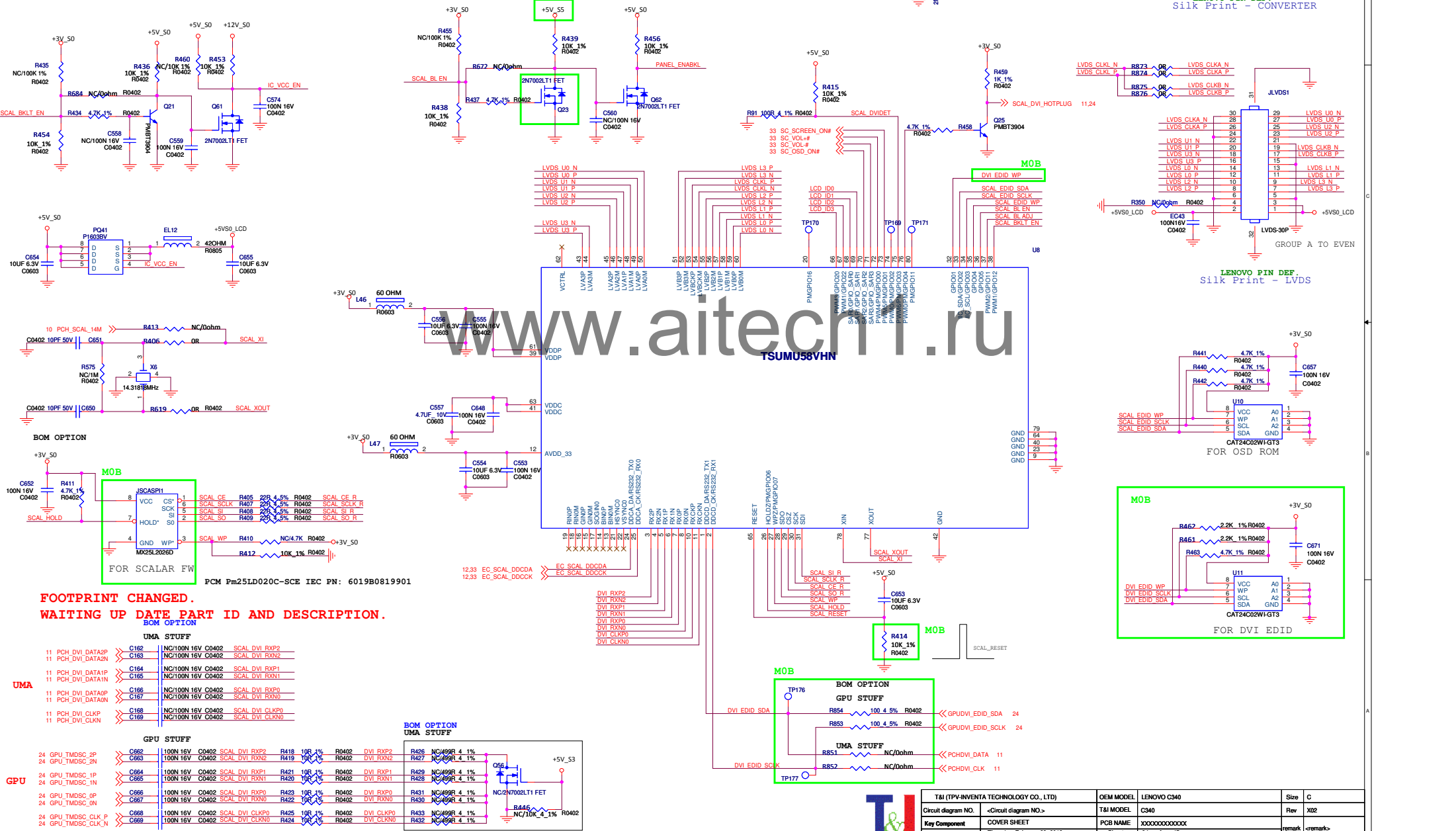
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Thursday, February 23, 2012	Sheet	30 of 45	remark

SCALAR TSUMU58VHN

Panel ID

SIZE	PANEL MODEL	ID3	ID2	ID1	ID0
21.5"	AUD M215H03 V1	1	1	1	1
	LG LM215HF4-TL61	1	1	0	1
	SEC LTM215HT04-M02	1	0	1	1
20"	CHI M215H02-L21	0	1	1	1
	AUD M200R01 V6	1	1	1	0
	LG LM200R03-TL61	1	1	0	0
	SEC LTM200R010-M01,M02	1	0	1	0
	CHI M200R02-L20	0	1	1	0

For SCALAR Panel ID



FOOTPRINT CHANGED.
WAITING UP DATE PART ID AND DESCRIPTION.

BOM OPTION

UMA	GPU	UMA STUFF	GPU STUFF
11 PHO_DVI_DATA2P	C162	NC/100N 16V C0402	SCAL DVI RXP2
11 PHO_DVI_DATA2N	C163	NC/100N 16V C0402	SCAL DVI RXN2
11 PHO_DVI_DATA1P	C164	NC/100N 16V C0402	SCAL DVI RXP1
11 PHO_DVI_DATA1N	C165	NC/100N 16V C0402	SCAL DVI RXN1
11 PHO_DVI_CLKP	C166	NC/100N 16V C0402	SCAL DVI RXP0
11 PHO_DVI_CLKN	C167	NC/100N 16V C0402	SCAL DVI RXN0
24 GPU_TMSDC_2P	C662	100N 16V C0402	SCAL DVI RXP2
24 GPU_TMSDC_2N	C663	100N 16V C0402	SCAL DVI RXN2
24 GPU_TMSDC_1P	C664	100N 16V C0402	SCAL DVI RXP1
24 GPU_TMSDC_1N	C665	100N 16V C0402	SCAL DVI RXN1
24 GPU_TMSDC_0P	C666	100N 16V C0402	SCAL DVI RXP0
24 GPU_TMSDC_0N	C667	100N 16V C0402	SCAL DVI RXN0
24 GPU_TMSDC_CLK_P	C668	100N 16V C0402	SCAL DVI CLKP0
24 GPU_TMSDC_CLK_N	C669	100N 16V C0402	SCAL DVI CLKN0



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	X02
Key Component	COVER SHEET	PCB NAME	X0000000000X	remark	<remark>
Date	Thursday, February 23, 2012	Sheet	34 of 45		

SYSTEM +3V_S5/+3V_S3/+3V_S0 +5V_S5/+5V_S3/+5V_S0

Pin to pin IC: RICHTEK--RT8223NZQW

Input A: 2.368A

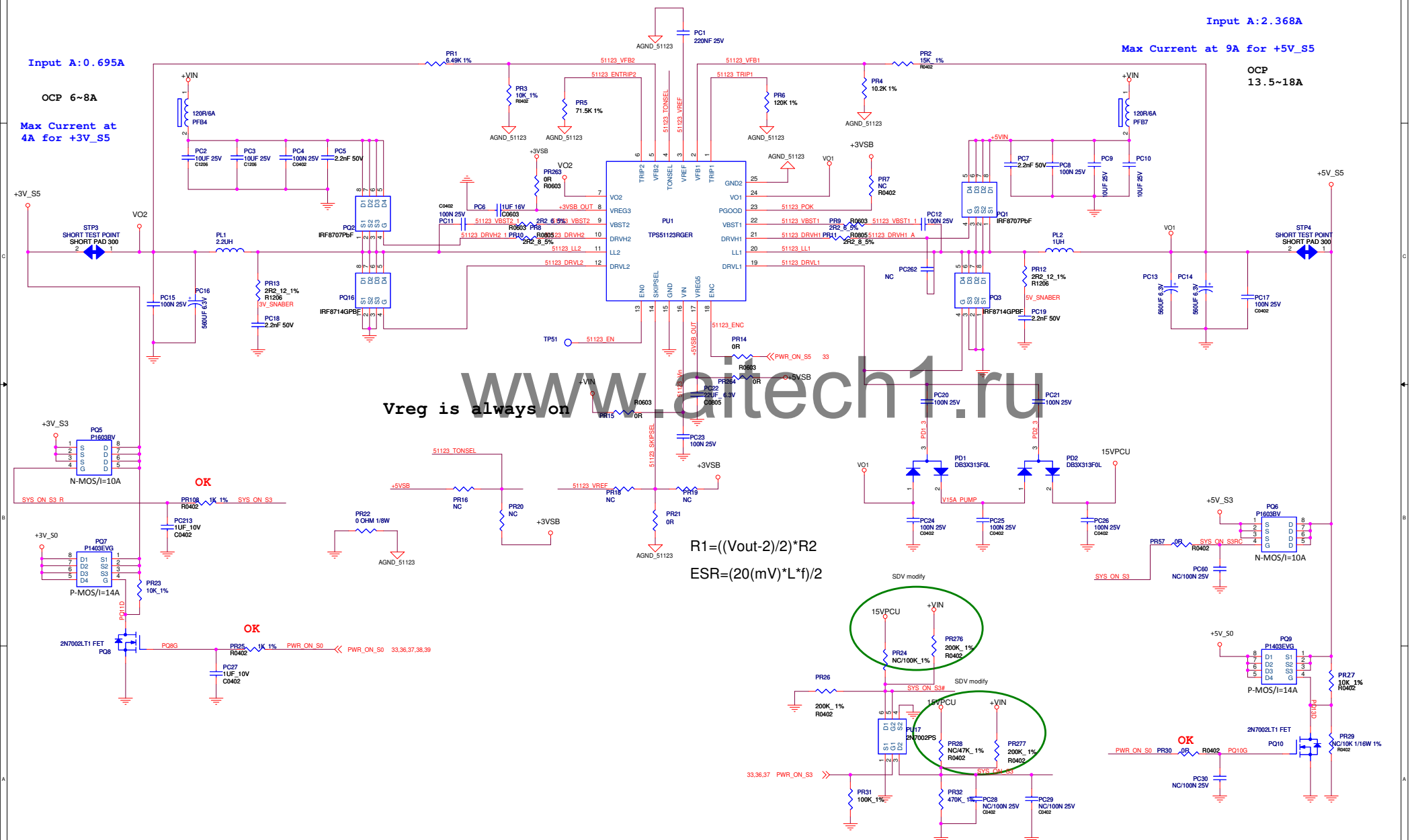
Max Current at 9A for +5V_S5

OCP 13.5~18A

Input A: 0.695A

OCP 6~8A

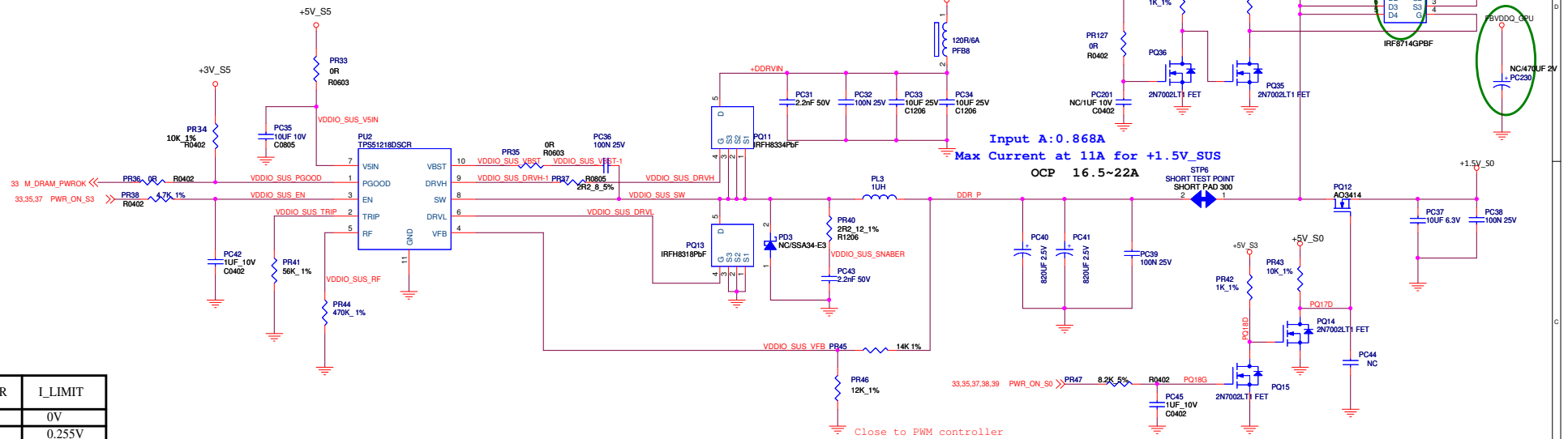
Max Current at 4A for +3V_S5



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev
COVER SHEET		PCB NAME	X000000000000	remark
Date	Thursday, February 23, 2012	Sheet	35 of 45	remark

+1.5V_SUS,VRM_1.5V,MEM_VTT,DC-IN

Pin to pin IC: RICHTEK--RT8237CZQW



Input A: 0.868A
Max Current at 11A for +1.5V_SUS
OCP 16.5~22A

Close to PWM controller

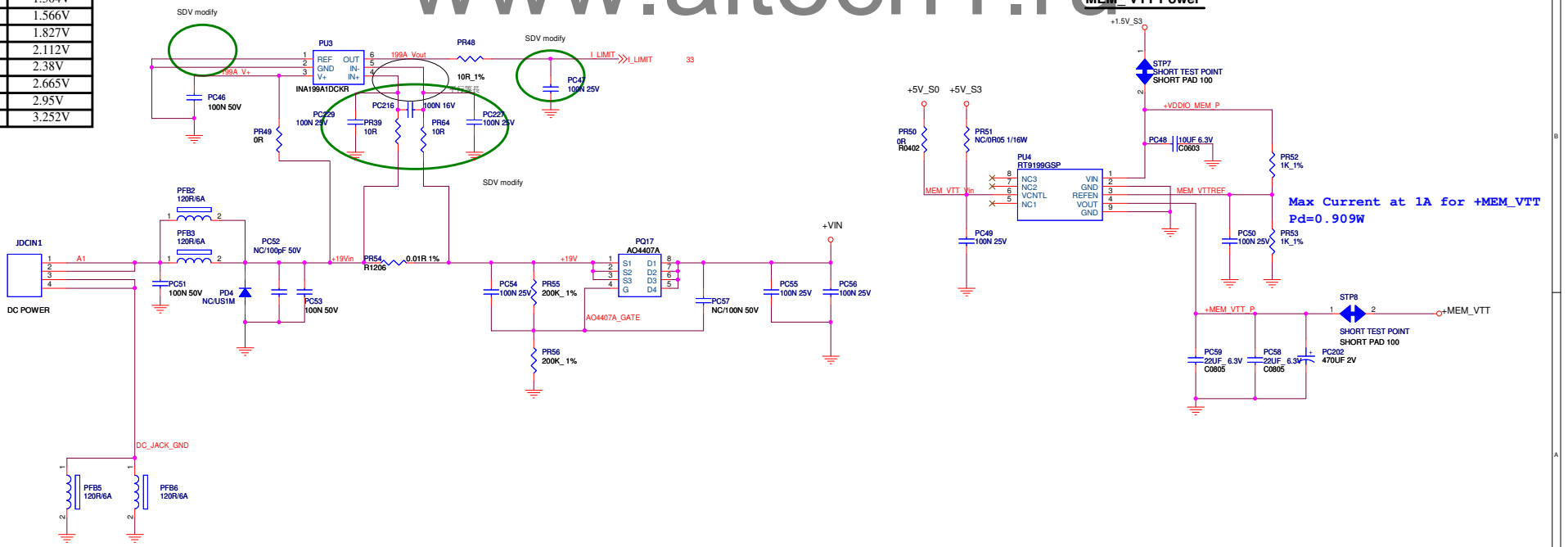
$$V_{out} = 0.704V * (R1 + R2) / R2$$

$$ESR = L * f / 70$$

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MEM_VTT Power

TOTAL POWER	I_LIMIT
0W	0V
10W	0.255V
20W	0.512V
30W	0.772V
40W	1.034V
50W	1.304V
60W	1.566V
70W	1.827V
80W	2.112V
90W	2.38V
100W	2.665V
110W	2.95V
120W	3.252V



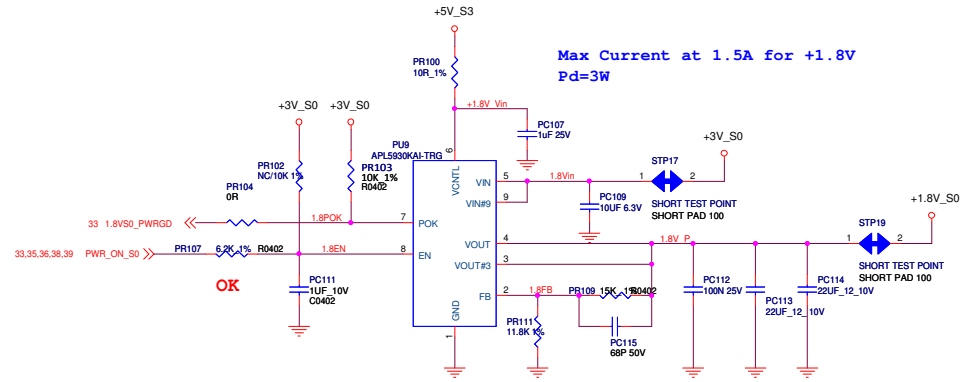
Max Current at 1A for +MEM_VTT
Pd=0.909W



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Thursday, February 23, 2012	Sheet	36 of 45	<remark>

+1.8V

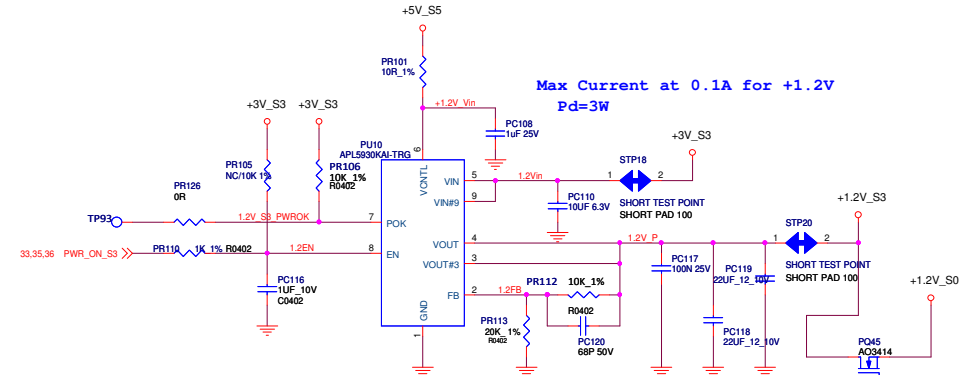
Max Current at 1.5A for +1.8V
Pd=3W



$$V_{out} = 0.8V \cdot (R1 + R2) / R2$$

+1.2V

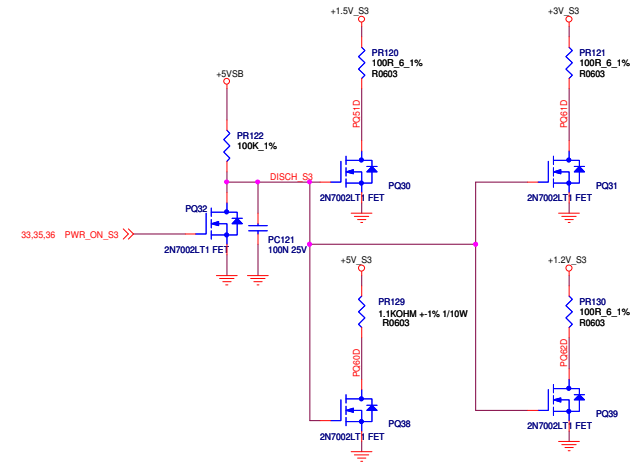
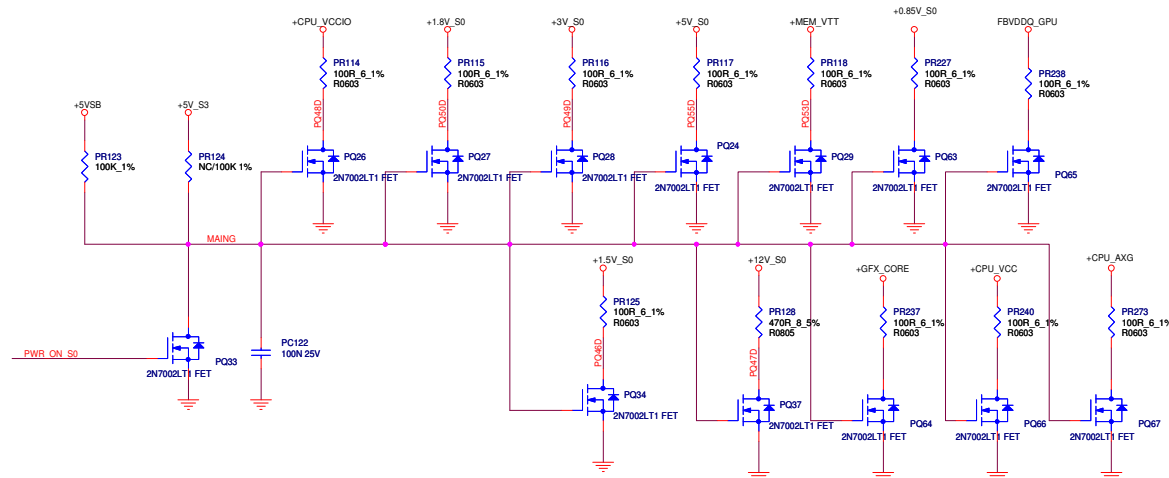
Max Current at 0.1A for +1.2V
Pd=3W



$$V_{out} = 0.8V \cdot (R1 + R2) / R2$$

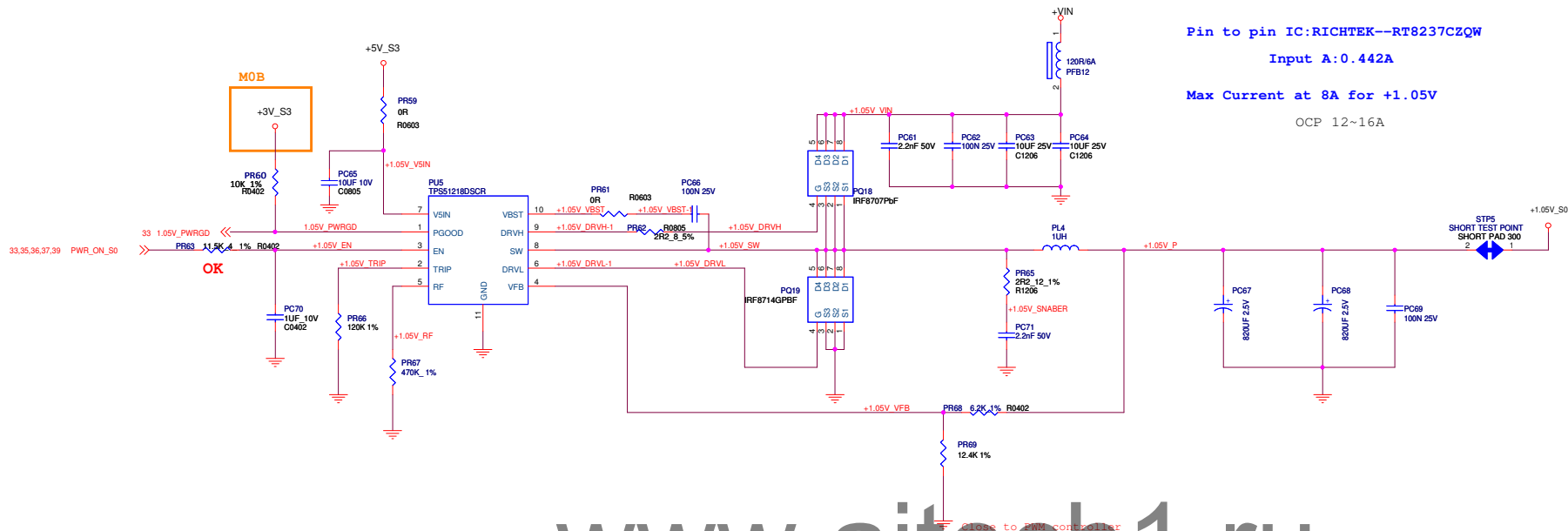
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DISCHARGE CIRCUIT



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	DEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev
COVER SHEET		PCB NAME	X000000000000	X02
Date	Thursday, February 23, 2012	Sheet	37 of 45	remark

+1.05V



Pin to pin IC: RICHTEK--RT8237CZQW

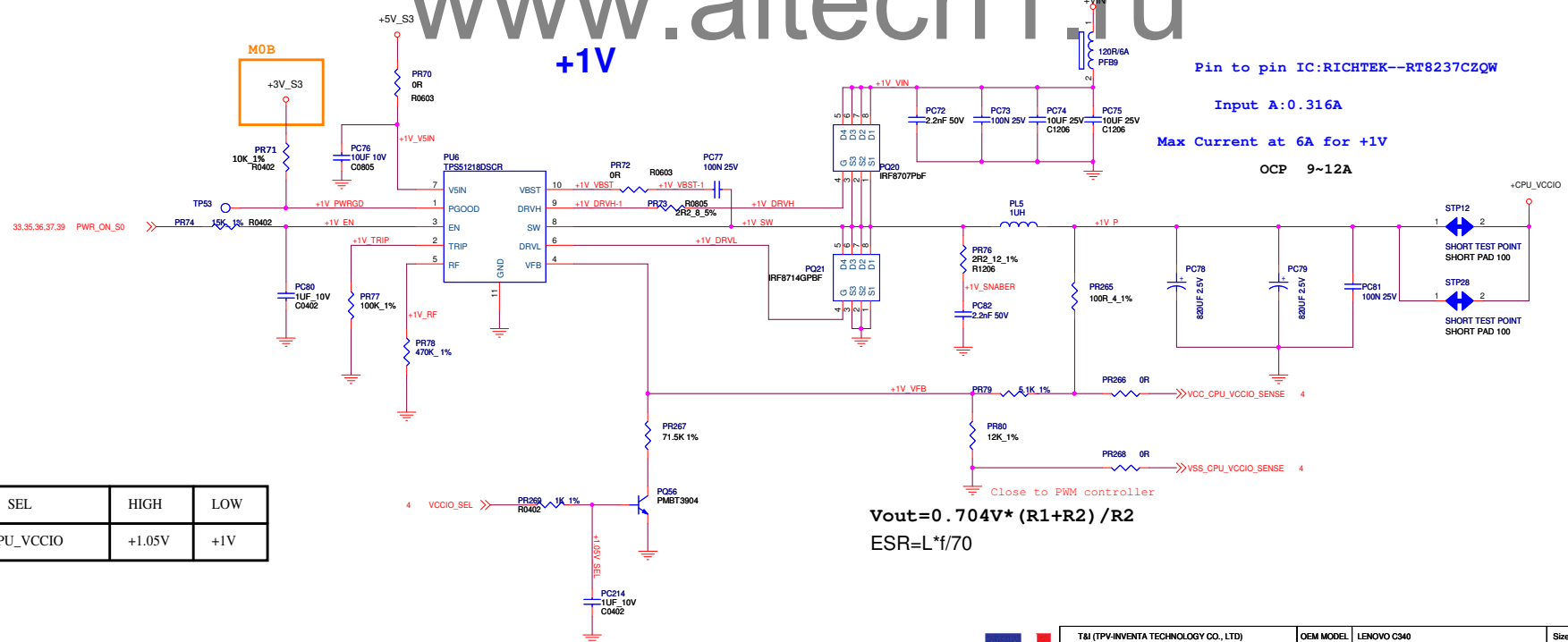
Input A: 0.442A

Max Current at 8A for +1.05V

OCP 12~16A

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+1V



Pin to pin IC: RICHTEK--RT8237CZQW

Input A: 0.316A

Max Current at 6A for +1V

OCP 9~12A

$$V_{out} = 0.704V * (R1 + R2) / R2$$

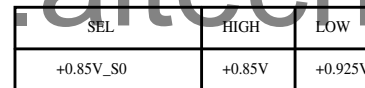
$$ESR = L * f / 70$$

SEL	HIGH	LOW
+CPU_VCCIO	+1.05V	+1V

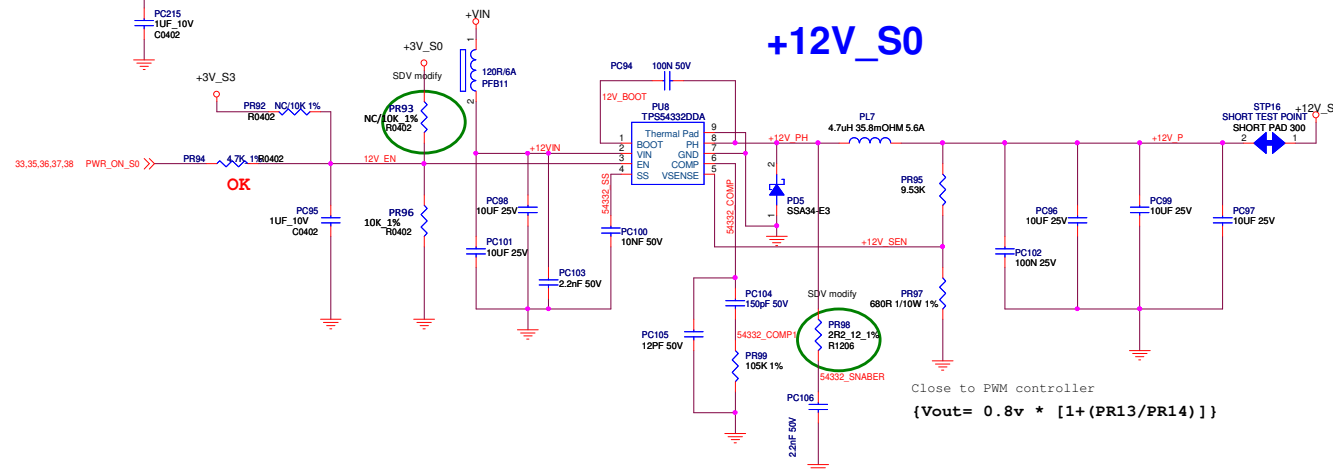


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Thursday, February 23, 2012	Sheet	38 of 45	<remark>

OCP 4.5A



Close to PWM controller

$$\{V_{out} = 0.8V * [1 + (PR13/PR14)]\}$$


PH0	PH1	# of PH
1	0	1
0	1	2
1	1	3



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	X02
Key Component	COVER SHEET	PCB NAME	X000000000000X	remark	<remark>
Date	Thursday, February 23, 2012	Sheet	42 of 45		

POWER SEQUENCE

Power ON

Power OFF

COIN BATTERY 3V

Net Name
RTC_BAT

RTC_RST

DC_IN

VIN = +19V

LDO OUT

+3VSB/+5VSB

POWER BTN to EC

SYS_PWRBTN#

PCH OUT TO EC (don't care)
PCH TO EC

PCH_SLP_SUS#

PCH OUT/IN

SUSWARN#&SUSACK#

EC OUT

PWR_ON_S5

POWER IC

+3V_S5/+5V_S5

EC OUT TO PCH

PCH_RSMRST#

EC OUT TO PCH

PCH_DPWR0K

EC TO PCH

PCH_PWR_BTN#

PCH TO EC

NC_SLP_S5_N

PCH TO EC

PCH_SLP_S4#

TP PCH_SLP_LAN#>PCH_SLP_A#

PCH OUT

PCH_SLP_S3#

EC OUT

PWR_ON_S3

POWER IC
& MOS

+3v_S3
+5V_S3
+1.5V_S3

S5 PWR

S3 PWR

S0 PWR

KBC OUT

PWR_ON_S0

+5V_S0/+3V_S0

OPTIONAL GPU

+1.05V_S0

+GFX_CORE

+1.5V_S0

PCH ALL POWER

+MEM_VTT

+12V_S0

+1.8V_S0

+1.2V_S0

+0.85V_S0

LOGIC TO EC

HW_PWRGD

EC TO PCH(APWROK)

PCH_APWR_OK

EC TO PCH

PCH_PWR_GD

EC TO VR PWR IC

CPU_PWR_EN

+CPU_VCC

+CPU_AXG

PWR TO KBC&PCH(SYS_PWROK)

CPU_PWR_GD

PCH TO CPU

H_DRAMPWRGD

PCH TO CPU

H_PWRGD

PCH TO ALL

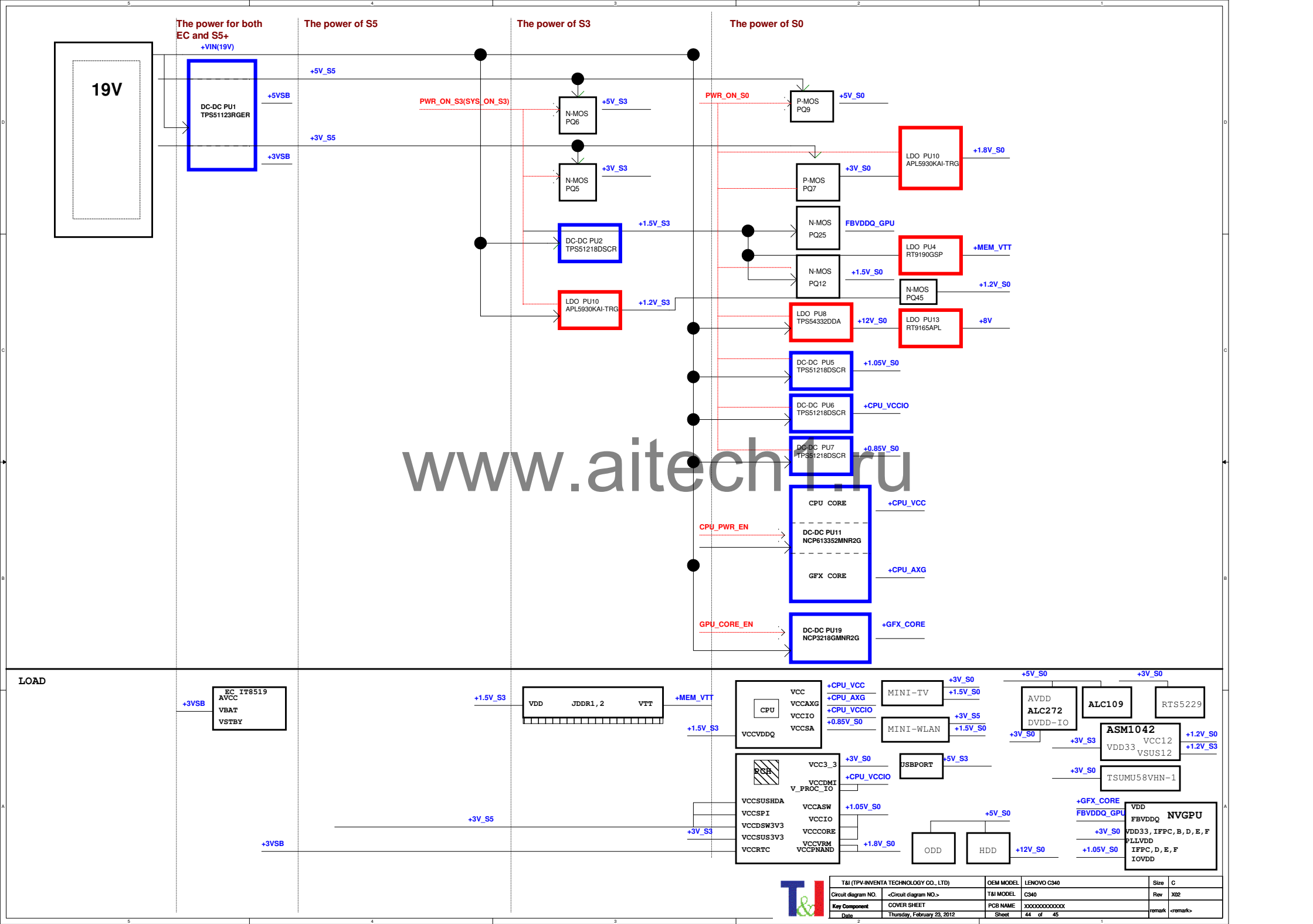
PLTRST_N

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T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Thursday, February 23, 2012	Sheet	43 of 45	<remark>

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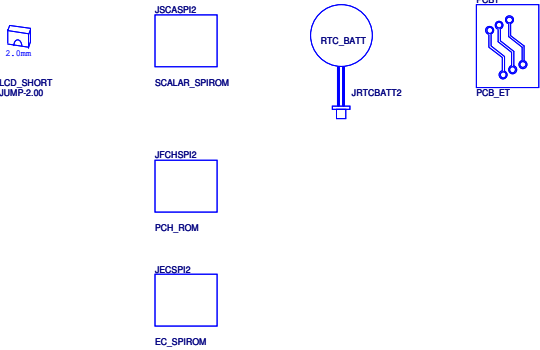


Schematic Modify History

5. PAGE 12. ADD R236 NC P/N
6. PAGE 16. ADD R352 NC P/N
8. PAGE 18. R325 CHANGE VALUE
16. PAGE 38. CORRECT 1.5V_S3 TO +3V_S3 ON PR60,PR71
17. PAGE 39. CORRECT 1.5V_S3 TO +3V_S3 ON PR82

01. PAGE 01. H30,H31 NC NUT PARTS,H32,H33,H34,H35 UPDATE NUT P/N.
02. PAGE 03. U1 INSTALL ,UPDATE P/N.
03. PAGE 12,30. CHANGE POWER NEAME FROM +3V_SPI_ROM TO +3V_SPI FOR SPI ROM
04. PAGE 30. DELETE Q76,C471 FOR +LAN_VDD33 POWER CIRCUIT
05. PAGE 30. RESERVE R464,R465,Q78 FOR +LAN_VDD33 DISCHARGE CIRCUIT
06. PAGE 11. RESERVE R158,R159 FOR BOARD ID, RESERVE R172~174 FOR VRAM ID
07. ADD C480 10uF C285 4.7uF FOR PEX_IOVDD, ADD C479 4.7uF FOR PEX_IOVDDQ
08. PAGE 17. R311 DEPOP
09. PAGE 24. SWAP GPU_TMDSC_ON/P, CHANGE GPU_SDA CONNECTOR TO U38.R5
11. PAGE 25. CHANGE LB7 VALUE TO 180 Ohm/100MHz, ADD C770 100nF
12. PAGE 31. RESERVE R516
13. PAGE 33. R717 ADD 2.2K FOR CIR_RX
13. PAGE 33. SCREEN_LED# CONNECTION CHANGE FROM U27 PIN 72 TO PIN 85

17. PAGE 33. DEL R613 PULL UP FOR EC_SCI#
18. PAGE 01. CHANGE H7~H9 FOOTPRINT.
19. PAGE 01. H20 AND H21 CHANGE FOOTPRINT.
20. PAGE 01. H22 CHANGE FOOTPRINT.
21. PAGE 31. R343 CHANGE PULL HIGH TO +5V_S3
22. PAGE 33. R625 DEPOP FOR Peci NO PULL UP
23. PAGE 10. EC_SCI CHANGE FROM PCH GPIO28 TO GPIO 10
24. PAGE 33. SCREEN_LED# CHANGE CONTROL PIN FROM U27 PIN 72 TO PIN 85
25. PAGE 33. R685 DEPOP FOR NVVDD_PWRGD
26. PAGE 34. R364 CHANGE VALUE FROM 100 Ohm TO 0 Ohm
27. PAGE 34. ADD R461,R462,R463,C671,U11 FOR PANEL EDID
28. PAGE 34. R414 CHANGE VALUE FROM 1K TO 10K FOR SCALA RESET
31. PAGE 34. R439 CHANGE TO +5V_S5 AND Q23 CHANGE FROM 3904 TO 2N7002 FOR FIX PANEL SEQUENCE
32. PAGE 30. RESERVE R466 FOR +3V_SPI



GPU SKU
29. PAGE 34. R853,R854 CHANGE VALUE FROM 0 Ohm TO 100 Ohm
30. PAGE 11. R764 DEPOP
33. PAGE 11. UMA R764 DEPOP

UMA SKU
29. PAGE 34. R851,R852 CHANGE VALUE FROM 0 Ohm TO 100 Ohm
30. PAGE 11. R764 ADD 0R FOR PCH DVI HPD
33. PAGE 11. UMA R764 POP 0 Ohm



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	X02
Key Component	COVER SHEET	PCB NAME	X00000000000X	remark	<remark>
Date	Thursday, February 23, 2012	Sheet	45 of 45		